IRT SAINT EXUPÉRY

Les Rendez-vous Fiabilite du CFF

Agenda.

Project FELINE

WP1: Component reliability (DSM and WBG)

- Failure mechanisms in DMS components
- Failure Risk Assessment Methodology (FRAME)
- Application of FRAME
- Smart reliability

WP4: Durability of SAC305 board-level assemblies

- Approach in solder durability assessment
- Thermal cycling [-55 ; 125]°C
- Finite element analyses
- Mechanical cycling

Conclusions

FELINE : Fiabilité ÉLectronique INtégrÉ

OBJECTIVES

- Développer et appliquer la méthodologie FRAME (Failure Risque Analysis Methododology) pour définir le niveau de risque des composants COTS en environnements opérationnels (PM)
- Traiter l'obsolescence des composants d'un point de vue CEM par l'utilisation de la simulation numérique
- Durabilité des assemblages des composants électroniques dans les applications petits signaux

6,9 M€

48 Mois (2017– 2021)

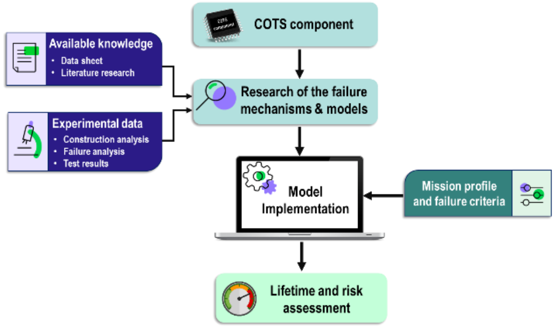
ACTIA, AIRBUS, AIRBUS DS, CONTINENTAL, ELEMCA, NEXIO, LIEBHERR, SAFRAN TECH, TECHFORM, THALES AV, THALES AS, TRAD, ZODIAC AEROSPACE

LAAS-CNRS, INSA Toulouse, IMS Bordeaux, IETR-CNRS, IES-CNRS

Lot 1

Fiabilité des COTS (DSM et WBG)

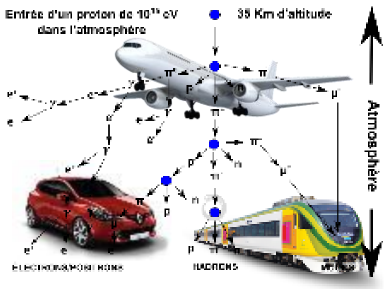
- Modélisation PoF des technologies DSM et GaN : TDDB, BTI, HCI et EM,
- Déploiement de l'approche FRAME,
- Plateforme de fiabilité SMART, Agile et simple d'utilisation.

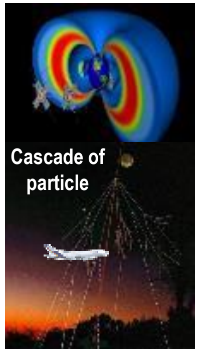


Lot 2

Radiation

- Comportement des récentes technologies à base de semi-conducteurs vis-à-vis des radiations cosmiques et atmosphériques : Ions lourds, Neutron, Proton et TID

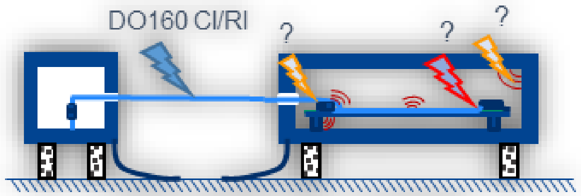




Lot 3

CEM

- Valider la non-régression des performances CEM d'un équipement face au changement d'un composant à partir de mesure sur composant / carte électronique :
  - ✓ La mesure d'émission en champ proche (NFSe),
  - ✓ La mesure d'immunité en champ proche (NFSi)

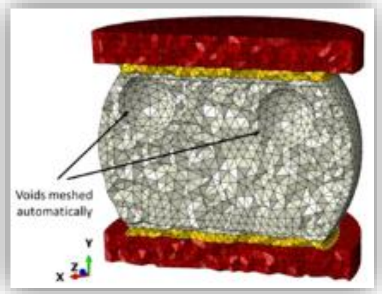


How to decline EMC constraints (DO160/CISPR) at Board or Component level?

Lot 4

Assemblage électronique

- Durabilité des carte électroniques faible puissance : fatigue mécanique des assemblages microélectroniques
- Modélisation multi-échelle : du joint de brasure à la carte équipée



Industrial **13**

PMEs **4**

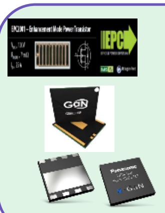
5 PhD (with 4 Laboratories)

5 Collaborations (3 international)

>15 Publications and Inudstrial Reports

WP2: RADIATION

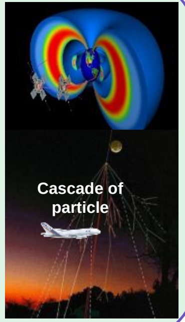
Definition of technologies and demonstrators



EPC	2045	100 V
EPC	2046	200 V
GaNSystems	GS1008P-E05-MR	100 V
GaNSystems	GS66508P-E05-MR	650 V
Panasonic	PGA26E07BA	600 V

Space (satellite & launchers)
→ Heavy Ions

Drone / helicopter / Aircraft
→ Neutron until 800MeV
→ Proton > 50 MeV



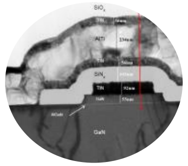
Radiative tests on WBG technologies

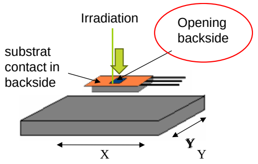
Bibliography

Characterization of immunity to radiations by X-ray & pulsed laser

PhD

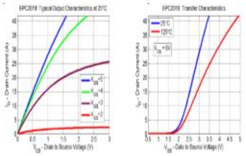
construction analysis



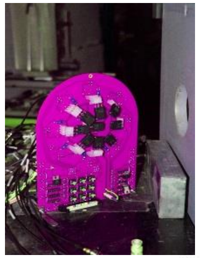


Component preparation

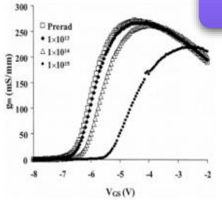
Electrical characterizations of components before testing



tests under radiative environment



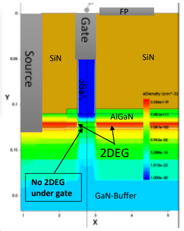
Electrical characterization of components after test



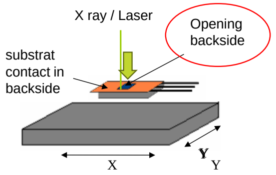
Modeling (Laser & X-rays

Experiments

TCAD simulation

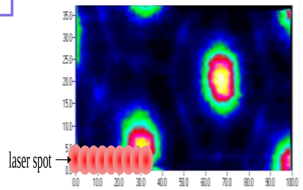


Sample preparation



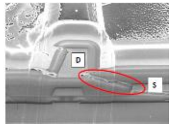
Laser testing

X-rays testing



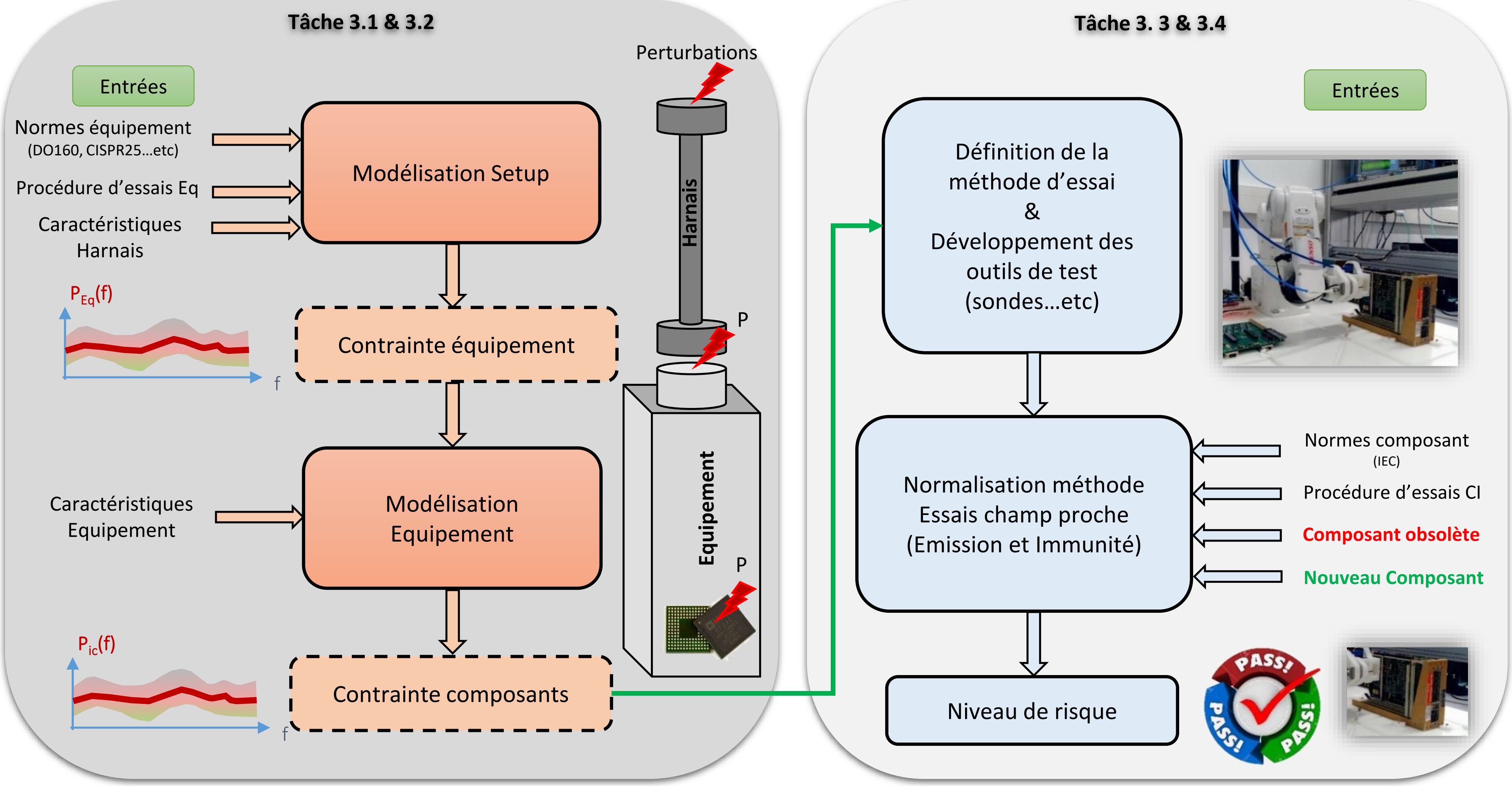
Data treatment of results

Failure Analysis



Contact : moustafa.zerarka@irt-saintexupery.com

Lot 3 : Gestion de l'obsolescence pour la CEM



Tâche 3.1 & 3.2

Entrées

Normes équipement (DO160, CISPR25…etc)

Procédure d'essais Eq

Caractéristiques Harnais

Modélisation Setup

Contrainte équipement

Caractéristiques Equipement

Modélisation Equipement

Contrainte composants

Tâche 3. 3 & 3.4

Entrées

Définition de la méthode d'essai & Développement des outils de test (sondes…etc)

Normalisation méthode Essais champ proche (Emission et Immunité)

Normes composant (IEC)

Procédure d'essais CI

Composant obsolète

Nouveau Composant

Niveau de risque

PhD N.N Au 01 Oct 2019 (IETR)

PhD S.CHETOUANI Au 01 Décembre 2017 (LAAS CNRS, INSA Toulouse)

PhD S.SERPAUD Au 01 Octobre 2018 (LAAS CNRS, INSA Toulouse)

PhD A. DURIER Au 01 Octobre 2018 (LAAS CNRS, INSA Toulouse, IMS)

FRENCH INSTITUTES OF TECHNOLOGY

Contact : sebastien.serpaud@irt-saintexupery.com

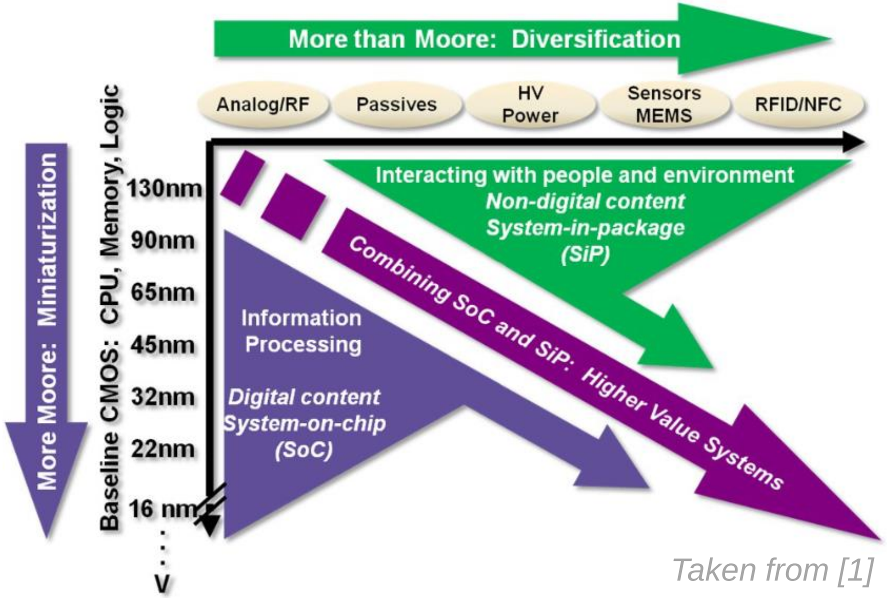
Work-package 1

Failure Risk Assessment Analysis for DSM and WBG components

Contact : valeria.rustichelli@irt-saintexupery.com

Semiconductor industry

- Markets demands for **performant components**:
  - ✓ High speed
  - ✓ Low power
  - ✓ Reduced cost → reduced size
- Semiconductor industry evolves quickly
  - ✓ **Technology complexity** is constantly increasing
  - ✓ **Time to market is reduce**



Taken from [1]

- What about reliability?

➢ Different **failure mechanisms** can affect the lifetime of an electronic component

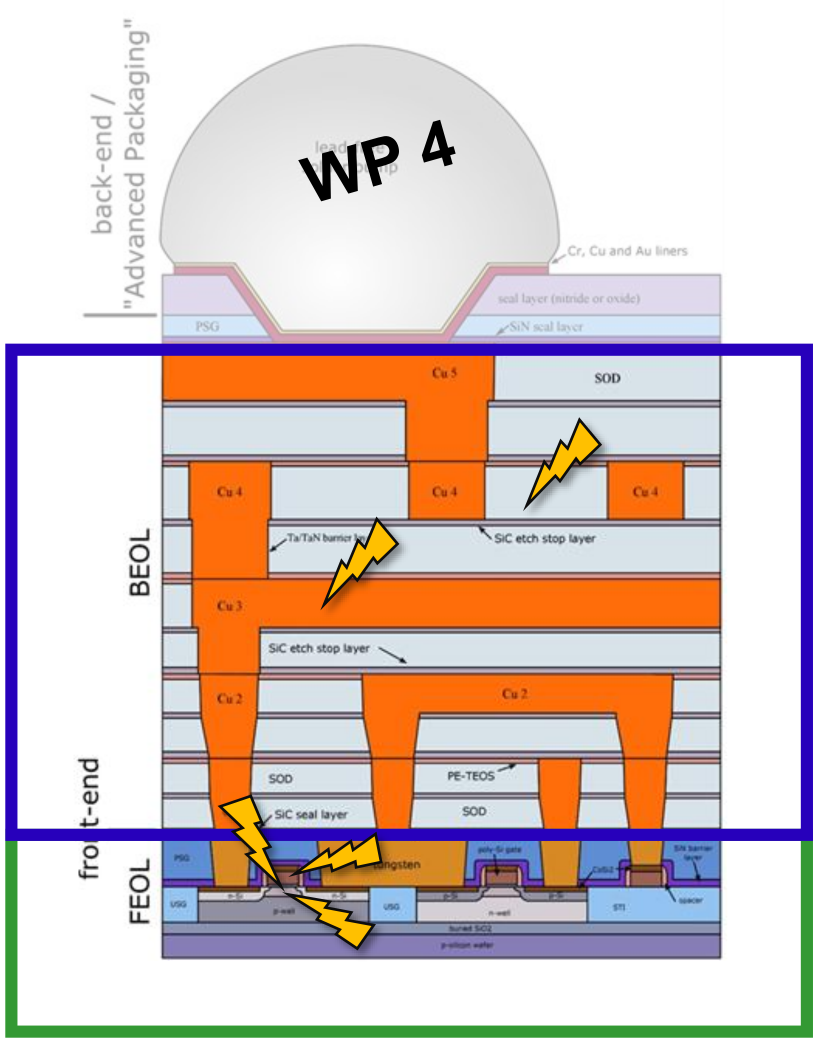
The goal of the **WP1** is to perform a **risk assessment analysis** based on **physics of failure (PoF)**

Failure Risk Assessment Methodology (FRAME)

- FRAME is a methodology based on the **physics of failure** of microelectronic components
- In **literature** there are several **physical failure models**
  - ➢ The models and their parameters depend on the **material** and the **geometry** of the component
- In this presentation we will focus on **failure** mechanisms of deep-submicron (**DSM**) component

- **What are the main failure mechanisms?**

Failure mechanisms in DSM component



Taken from [2]

➢ BEOL:

- Time Dependent Dielectric Breakdown
- Electromigration

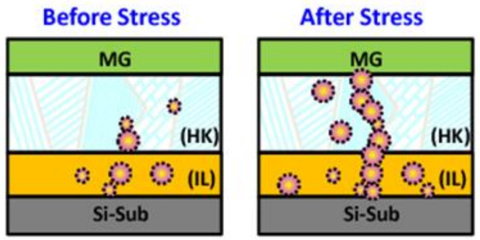
➢ FEOL:

- Time Dependent Dielectric Breakdown
- Bias temperature instability
- Hot carrier injection

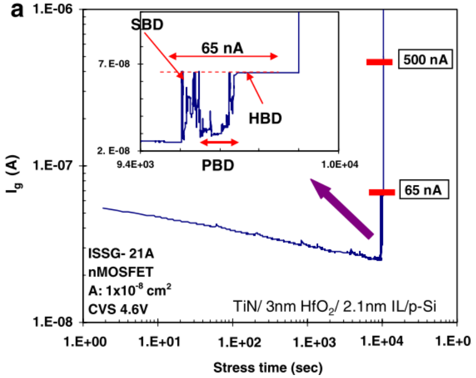
DSM failure mechanisms

TDDB

- Time Dependent Dielectric breakdown



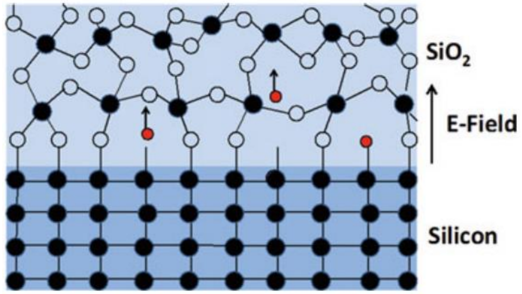
Taken from [3]



Taken from [4]

BTI

- Bias Temperature Instability



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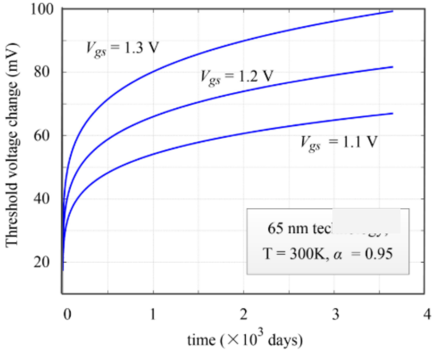
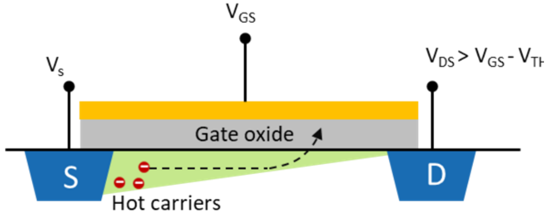
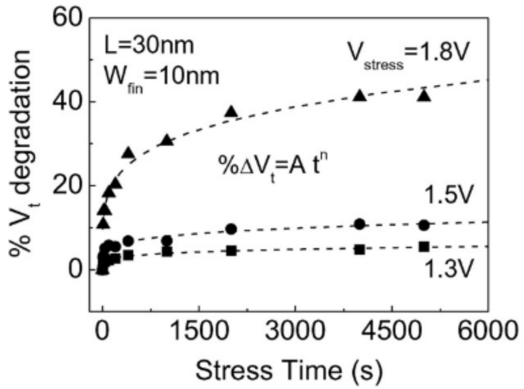


Taken from [6]

HCI

- Hot Carrier Injection

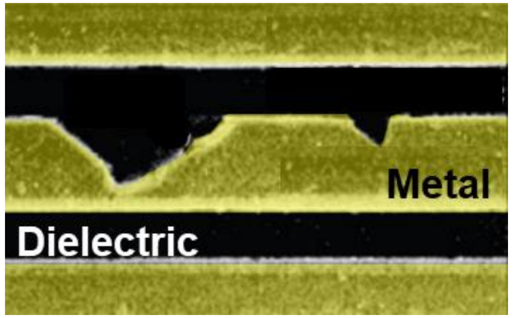




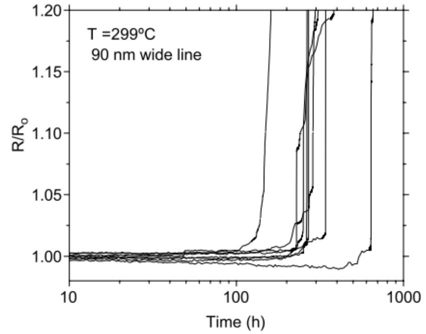
Taken from [7]

EM

- Electromigration

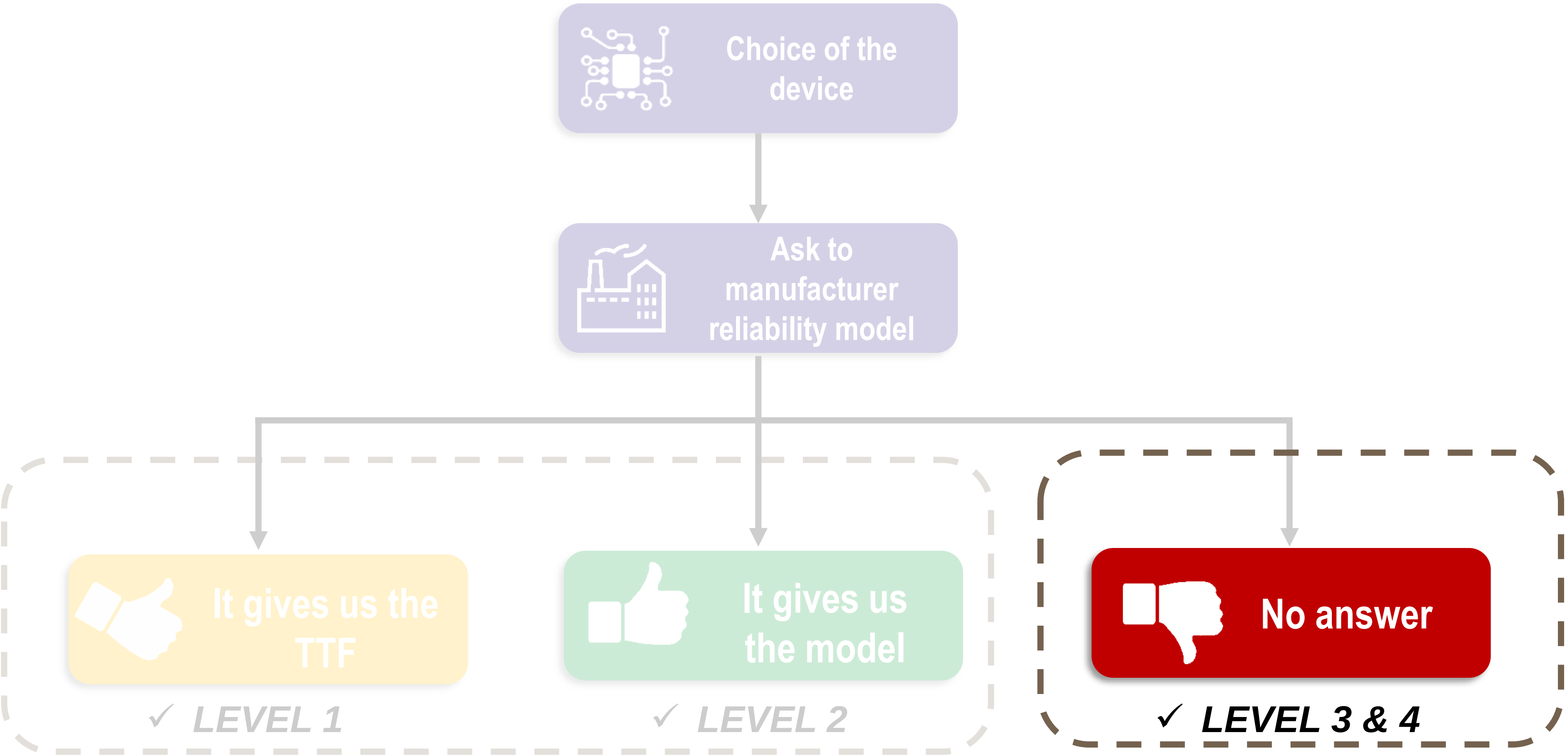


Taken from [8]



Taken from [9]

FRAME



Choice of the device

Ask to manufacturer reliability model

It gives us the TTF

✓ LEVEL 1

It gives us the model

✓ LEVEL 2

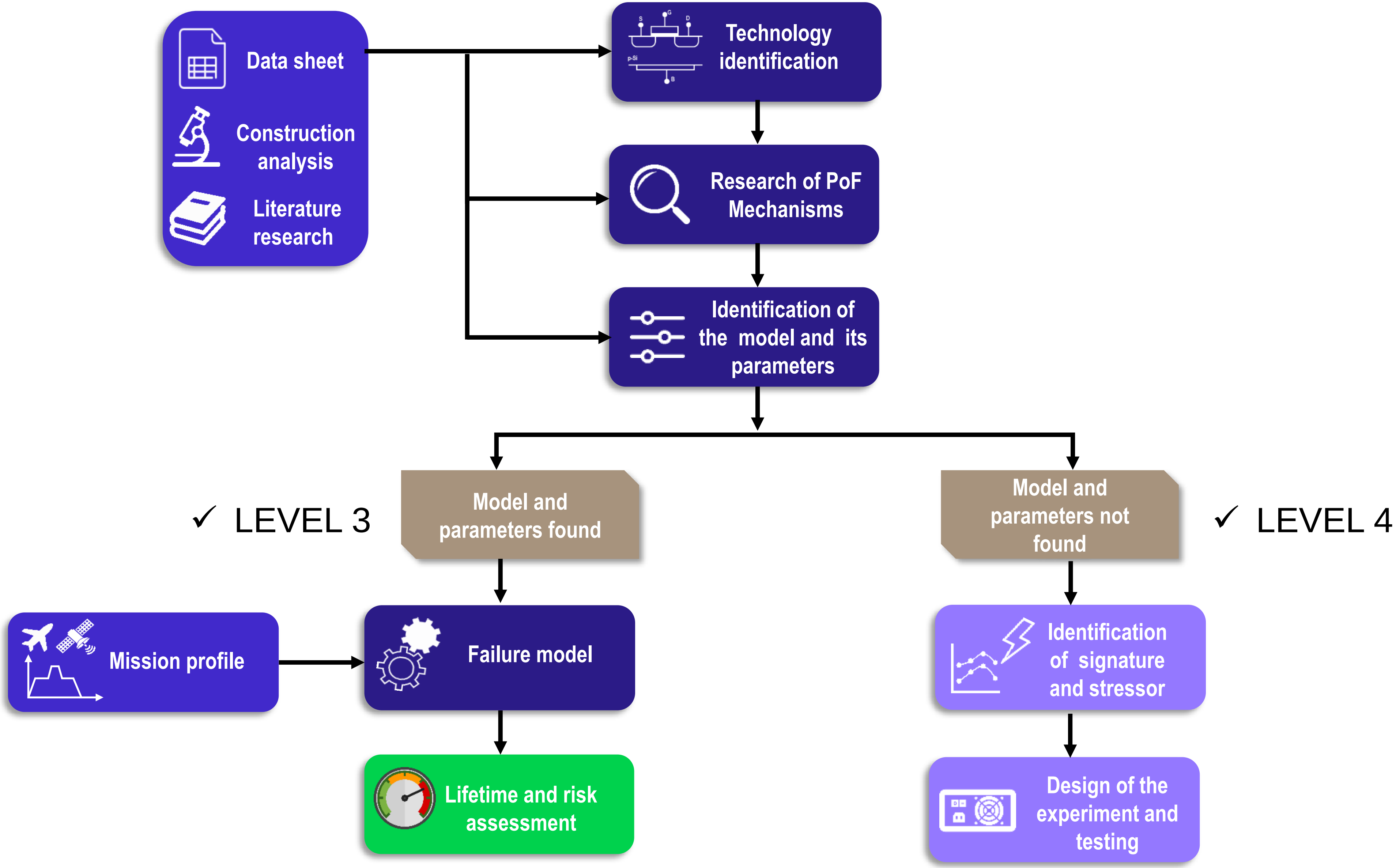
No answer

✓ LEVEL 3 & 4

It doesn't happen often

More luckily

FRAME



Data sheet

Construction analysis

Literature research

Technology identification

Research of PoF Mechanisms

Identification of the model and its parameters

✓ LEVEL 3

Model and parameters found

Mission profile

Failure model

Lifetime and risk assessment

Model and parameters not found

✓ LEVEL 4

Identification of signature and stressor

Design of the experiment and testing

From the publication to the lifetime estimation

In the **publication** lifetime values (TTF), come from **stressed tests**:

- High temperatures
- High voltages

This is necessary to observe a failure

TTF_{pub} is known

In the **real application,** usage conditions are different:

- “Normal” temperature
- “Normal” voltages

These are defined in the mission profile

$TTF_{app} = ?$

$$TTF_{app} = AF_V \cdot AF_T \cdot TTF_{pub}$$

AF_V: voltage acceleration factor
AF_T: temperature acceleration factor

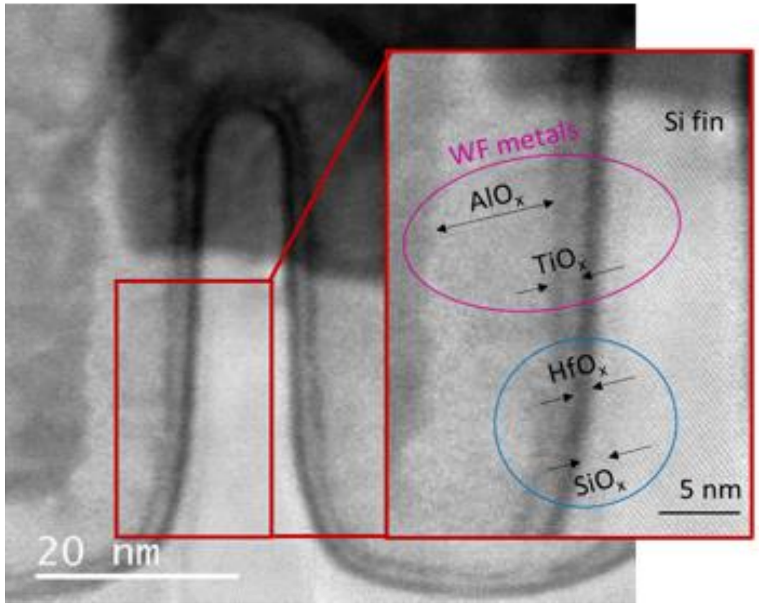
→ Their values depend on the **material** and the **geometry** of the device

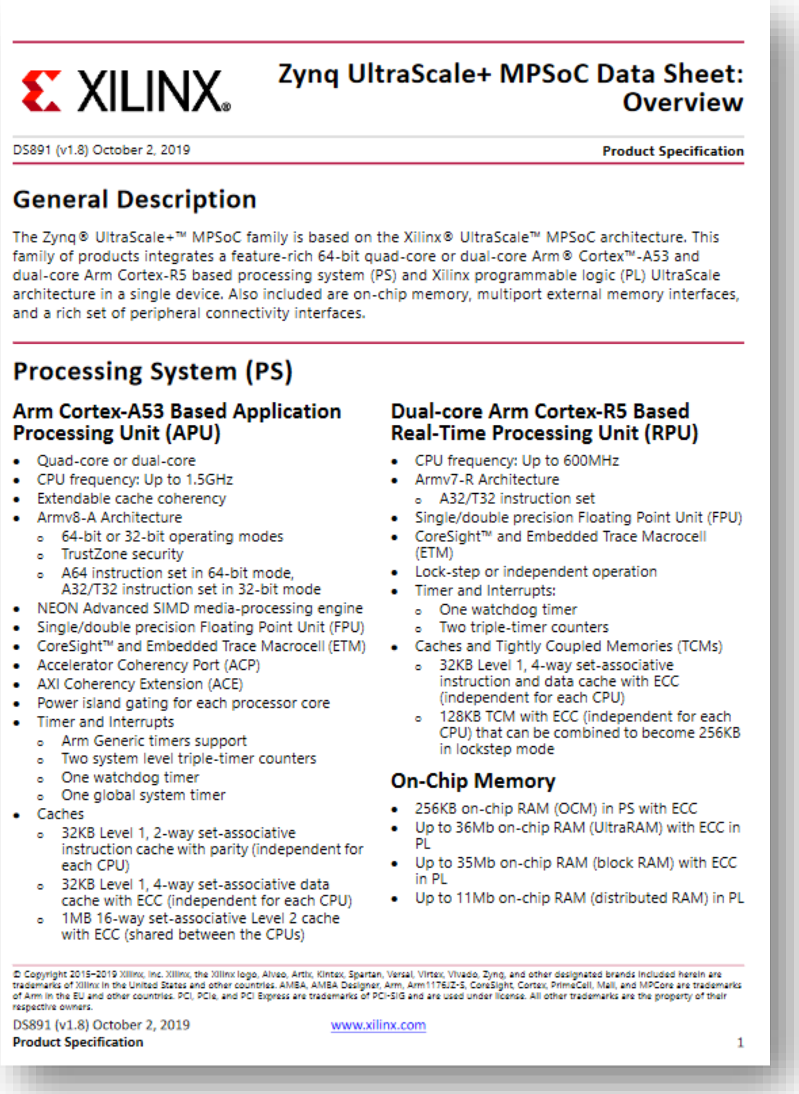
Application of FRAME: an example (TDDB on a FPGA)

FRAME

Data sheet

Construction analysis





XILINX

Zynq UltraScale+ MPSoC Data Sheet: Overview

DS891 (v1.8) October 2, 2019 **Product Specification**

General Description

The Zynq® UltraScale+™ MPSoC family is based on the Xilinx® UltraScale™ MPSoC architecture. This family of products integrates a feature-rich 64-bit quad-core or dual-core Arm® Cortex™-A53 and dual-core Arm Cortex-R5 based processing system (PS) and Xilinx programmable logic (PL) UltraScale architecture in a single device. Also included are on-chip memory, multiport external memory interfaces, and a rich set of peripheral connectivity interfaces.

Processing System (PS)

Arm Cortex-A53 Based Application Processing Unit (APU)

- Quad-core or dual-core
- CPU frequency: Up to 1.5GHz
- Extendable cache coherency
- Armv8-A Architecture
  - 64-bit or 32-bit operating modes
  - TrustZone security
  - A64 instruction set in 64-bit mode, A32/T32 instruction set in 32-bit mode
- NEON Advanced SIMD media-processing engine
- Single/double precision Floating Point Unit (FPU)
- CoreSight™ and Embedded Trace Macrocell (ETM)
- Accelerator Coherency Port (ACP)
- AXI Coherency Extension (ACE)
- Power island gating for each processor core
- Timer and Interrupts
  - Arm Generic timers support
  - Two system level triple-timer counters
  - One watchdog timer
  - One global system timer
- Caches
  - 32KB Level 1, 2-way set-associative instruction cache with parity (independent for each CPU)
  - 32KB Level 1, 4-way set-associative data cache with ECC (independent for each CPU)
  - 1MB 16-way set-associative Level 2 cache with ECC (shared between the CPUs)

Dual-core Arm Cortex-R5 Based Real-Time Processing Unit (RPU)

- CPU frequency: Up to 600MHz
- Armv7-R Architecture
  - A32/T32 instruction set
- Single/double precision Floating Point Unit (FPU)
- CoreSight™ and Embedded Trace Macrocell (ETM)
- Lock-step or independent operation
- Timer and Interrupts:
  - One watchdog timer
  - Two triple-timer counters
- Caches and Tightly Coupled Memories (TCMs)
  - 32KB Level 1, 4-way set-associative instruction and data cache with ECC (independent for each CPU)
  - 128KB TCM with ECC (independent for each CPU) that can be combined to become 256KB in lockstep mode

On-Chip Memory

- 256KB on-chip RAM (OCM) in PS with ECC
- Up to 36Mb on-chip RAM (UltraRAM) with ECC in PL
- Up to 35Mb on-chip RAM (block RAM) with ECC in PL
- Up to 11Mb on-chip RAM (distributed RAM) in PL

DS891 (v1.8) October 2, 2019 www.xilinx.com
Product Specification 1

For the TDDB we need to know:

- Temperature: depends on MP
- V_{app}: 0,85 V
- Gate oxide
  - Nature: SiO_2
  - Area: 2,83 E-3 μm^2

Application of FRAME: an example (TDDB on a FPGA)

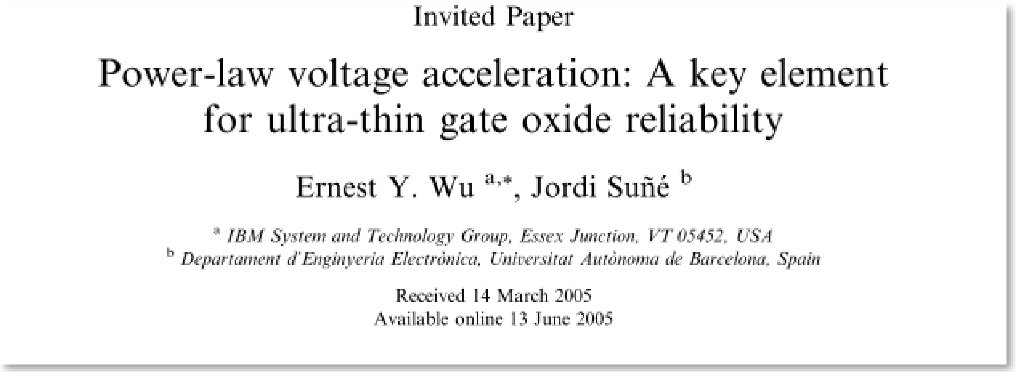
FRAME

Data sheet

Construction analysis

Literature research

- Thanks to the construction analysis we know that the gate dielectric is SiO_2
- Which model to use ? **Literature review**



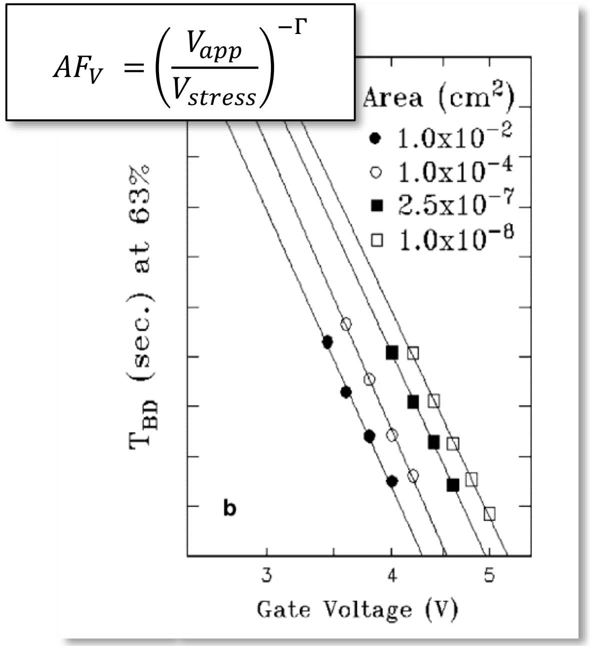
Invited Paper

Power-law voltage acceleration: A key element for ultra-thin gate oxide reliability

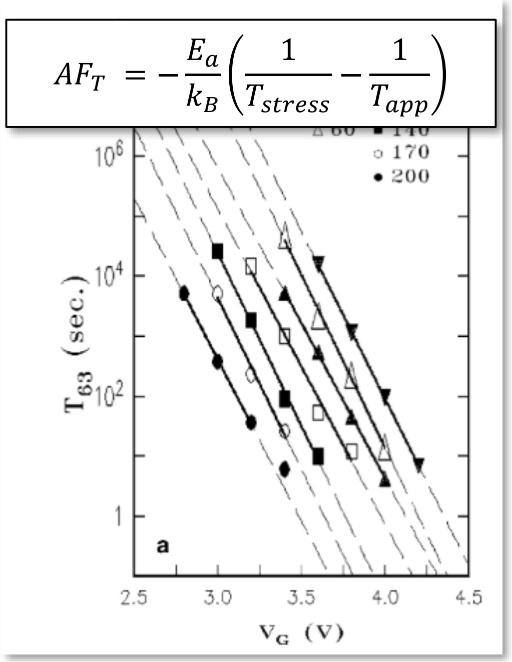
Ernest Y. Wu [a,*], Jordi Suñé [b]

[a] IBM System and Technology Group, Essex Junction, VT 05452, USA
[b] Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Spain

Received 14 March 2005
Available online 13 June 2005

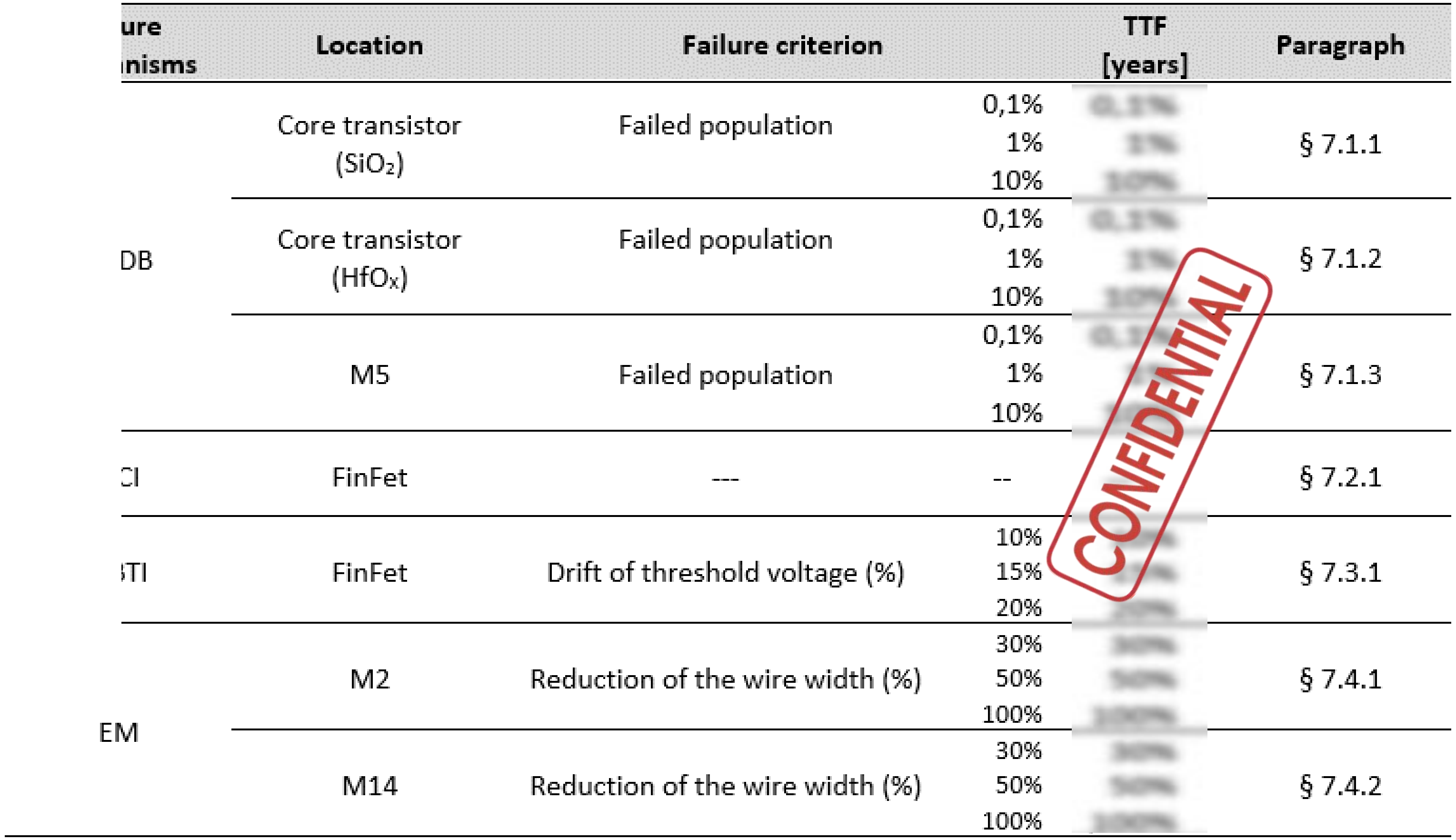


$$AF_V = \left(\frac{V_{app}}{V_{stress}}\right)^{-\Gamma}$$



$$AF_T = -\frac{E_a}{k_B}\left(\frac{1}{T_{stress}} - \frac{1}{T_{app}}\right)$$

Example of application: FPGA Xilinx



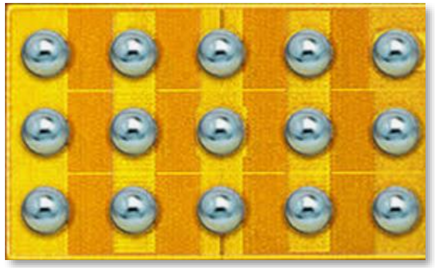
ure nisms	Location	Failure criterion		TTF [years]	Paragraph
DB	Core transistor (SiO$_2$)	Failed population	0,1%	[redacted]	§ 7.1.1
			1%	[redacted]	
			10%	[redacted]	
	Core transistor (HfO$_x$)	Failed population	0,1%	[redacted]	§ 7.1.2
			1%	[redacted]	
			10%	[redacted]	
	M5	Failed population	0,1%	[redacted]	§ 7.1.3
			1%	[redacted]	
			10%	[redacted]	
CI	FinFet	---	--		§ 7.2.1
TI	FinFet	Drift of threshold voltage (%)	10%	[redacted]	§ 7.3.1
			15%	[redacted]	
			20%	[redacted]	
EM	M2	Reduction of the wire width (%)	30%	[redacted]	§ 7.4.1
			50%	[redacted]	
			100%	[redacted]	
	M14	Reduction of the wire width (%)	30%	[redacted]	§ 7.4.2
			50%	[redacted]	
			100%	[redacted]	

CONFIDENTIAL

Table 22 Summary of the FRAME analysis on the FPGA component (aeronautic mission profile).

Successful application of FRAME

- FRAME can be applied to any electronic component, for example:
  - **Deep-submicron (DSM) digital components:**
    - FPGAs:
      - Xilinx XCZU9EG
      - PolarFire MPF300TFCG4841930K1A2N1IS KOR
    - Memories
      - DDR3 MT41K256M16TW-107-AAT.P
      - DDR4 MT 40 A 512M16 LY 062 E 1Ynm
  - **WBG components:**
    - GaN:
      - GaN FET 100 V: EPC2045
    - SiC:
      - SiCRET project: SCTW40N120-xxxx



SMART Reliability

Need of **capitalization**:

- ➢ Creation of database of all the analysed devices

Need of a **user-friendly** interface

- ➢ The final user has to be able to just "play" with the mission profile; no need to know the model behind

Need of **security**

- ➢ The mission profile is an extremely sensible information

Development of a new software: **Smart Reliability©** in collaboration with TECHFORM

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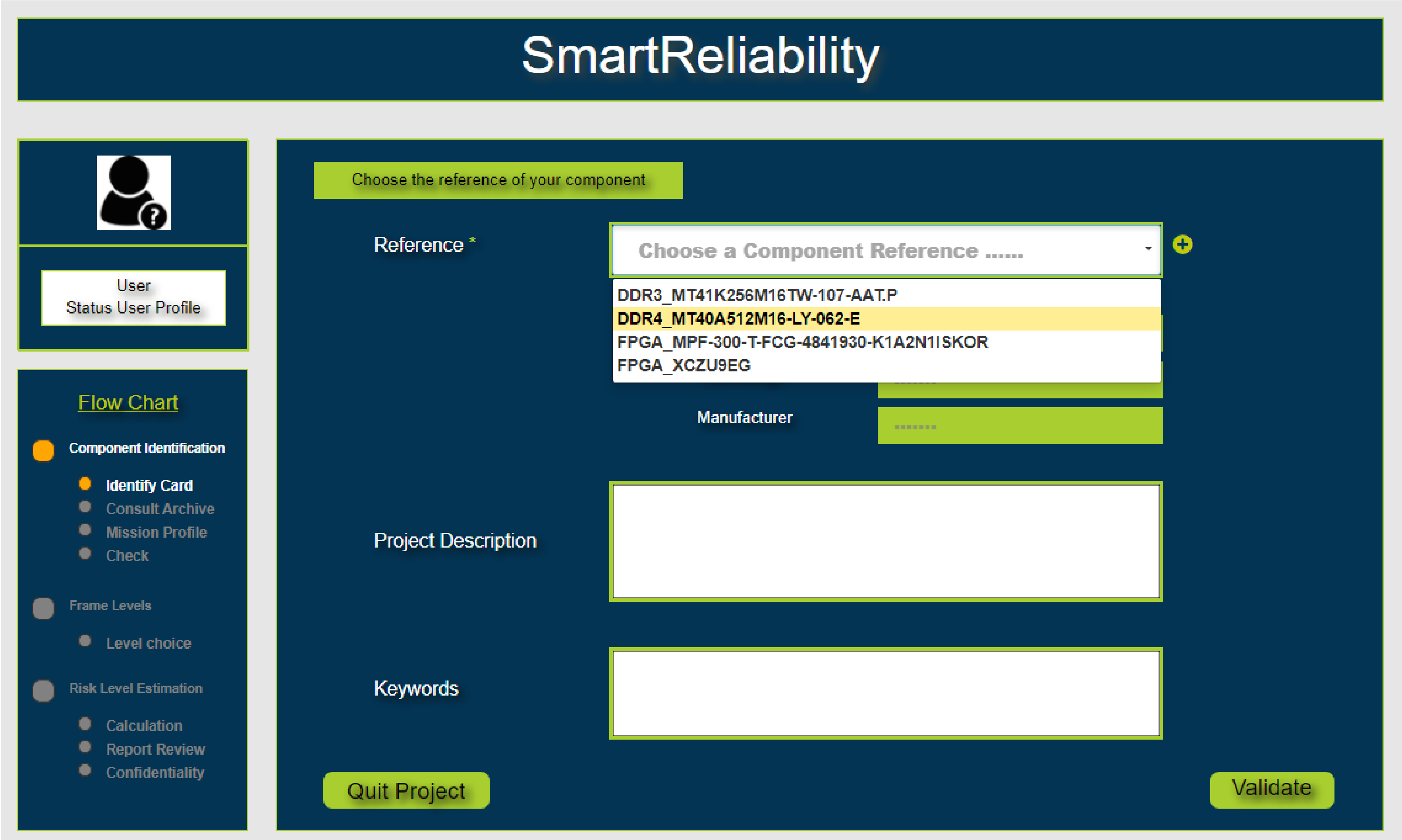
SMART Reliability



SmartReliability

User
Status User Profile

Flow Chart

- Component Identification
  - Identify Card
  - Consult Archive
  - Mission Profile
  - Check
- Frame Levels
  - Level choice
- Risk Level Estimation
  - Calculation
  - Report Review
  - Confidentiality

Choose the reference of your component

Reference * Choose a Component Reference ......

- DDR3_MT41K256M16TW-107-AAT.P
- DDR4_MT40A512M16-LY-062-E
- FPGA_MPF-300-T-FCG-4841930-K1A2N1ISKOR
- FPGA_XCZU9EG

Manufacturer ....

Project Description

Keywords

Quit Project

Validate

SMART Reliability

admin admin
Sample User

Your Actuel project is a Frame Level Three Case

FPGA_MPF-300-T-FCG-4841930-K1A2N1ISKOR

SMART Reliability

Your Actuel project is a Frame Level Three Case

DDR4_MT40A512M16-LY-062-E

Physics Of Failure Model: EM 2 : Copper, line M3

Model Parameters

ρ (Ω.m) :	3,50E-08
j (A.m^{-2}) :	1,50E+10
δ_s (m) :	5,00E-10
w (m) :	2,48E-07
h (m) :	2,14E-07
D_0 (m^2.s^{-1}) :	2,60E-05
Z_{eff}^* :	8,00E-01
σ_c (Pa) :	4,00E+08
σ_0 (Pa) :	3,00E+08
Ω (m^3) :	1,18E-29
E_a (eV)	9,00E-01
B (Pa)	3,00E+10

Model parameters

Mission Profile

T_{appl} (on)	Temperature (°C)	Duration (hour)
Phase N° 1	40	700
Phase N° 2	55	1400

T_{appl} (off)	Temperature (°C)	Duration (hour)
Phase N° 5	15	1830

ΔT (°C): 4

Failure Criterion

Δw (%): 10

Mission profile + Failure criteria

Calculate: 1,32E+02

Lifetime calculation

Conclusions

- ✓ FRAME has bees successfully applied on four different DSM components
- ✓ FRAME has bees successfully applied on SiC component (SiCRET project)
- ✓ FRAME is being applied to a GaN transistor from EPC
- ✓ SMART reliability allowed the capitalization of the analysed components

What is next…

- **Presentation of SMART reliability** @ Areospace valley webinar (date tbd)
- **Presentation of FRAME:**
  - NRTW conference (13-14 October) at IRT - Toulouse
- **Workshops:**
  - HCI physics with prof. A. Bravaix (May 2021)
  - GaN failure mechanisms with prof. Meneghini and Meneghesso at the University of Padova (date to be defined)
- **Application of FRAME to other projects :**
  - SiCRET
  - GaNRET

Work-package 4

Durability of SAC305 board-level assemblies

Contact : pierre.roumanille@irt-saintexupery.com

Motivation & background

- **Pb-free** solders since 2006 : SnAgCu alloys used in surface mount assemblies

- **Solder failure** by (thermo)mechanical fatigue :
  - Depends on SAC **initial microstructure**
  - Strong relationship with **microstructure evolution**

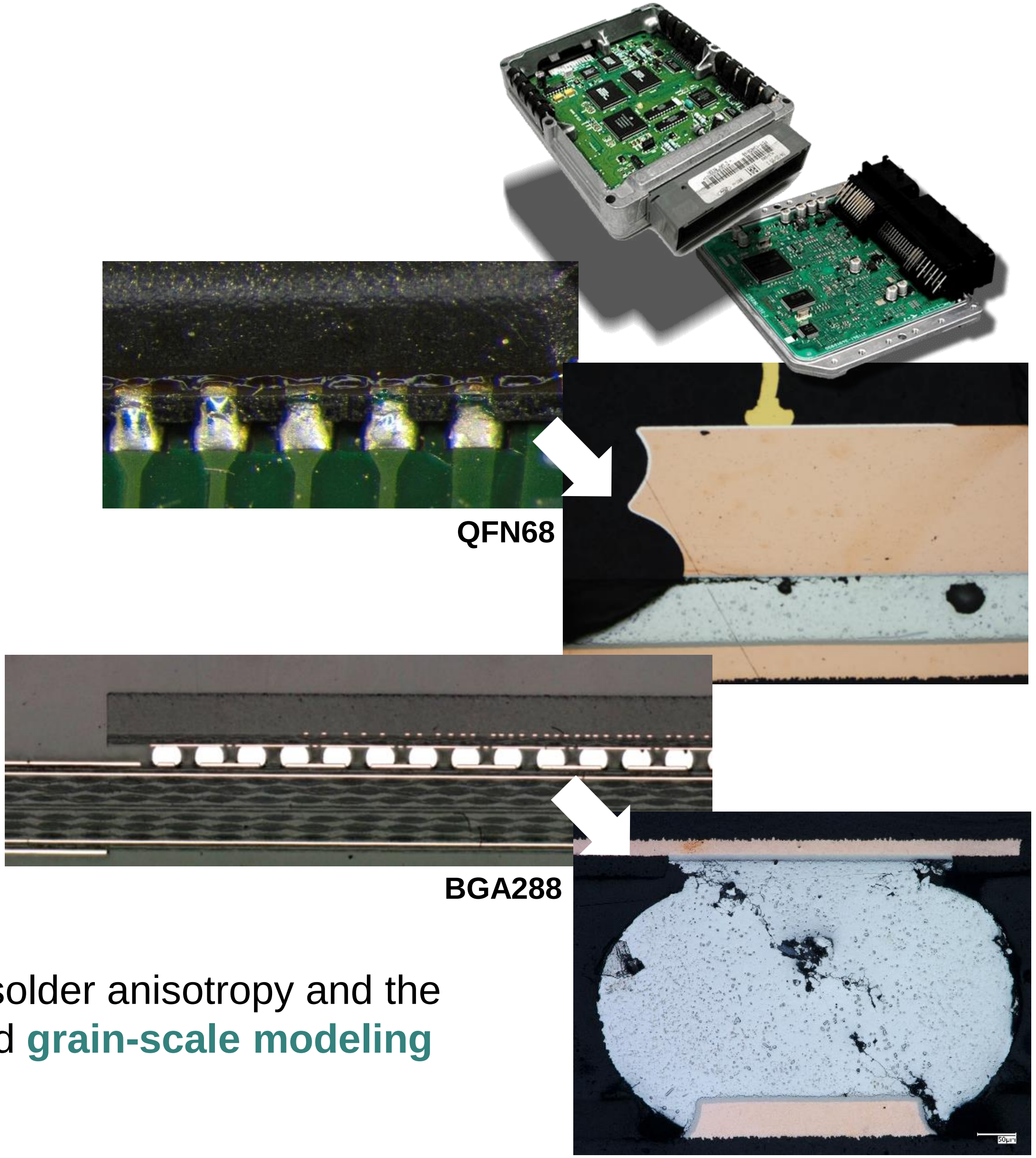
- Need more accurate description of the solder **failure mechanism**

- Need better **damage metrics and fatigue models** that consider the impact of solder microstructure for :
  - Design and virtual testing
  - Acceleration models

$$X = K(N)^c$$

Fatigue criterion

Cycles to failure



The goal of the **WP4** is to take into account the solder anisotropy and the microstructure evolution for **failure analysis** and **grain-scale modeling**

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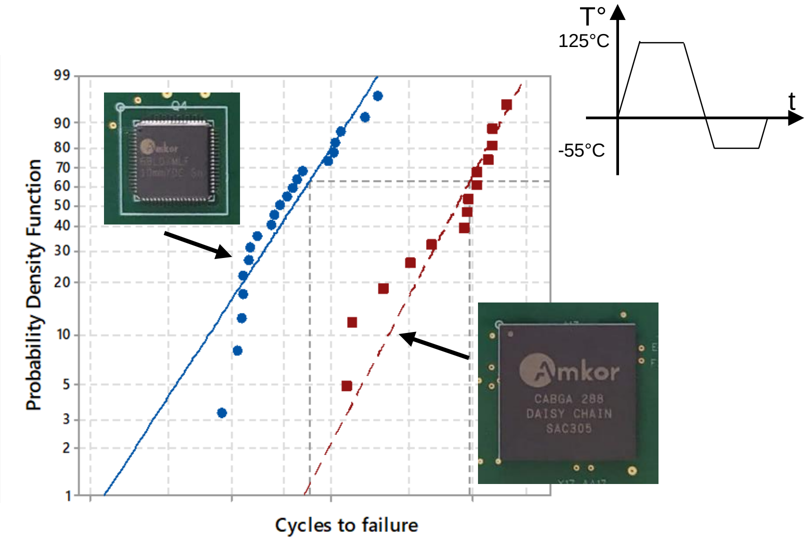
Approach in solder durability assessment



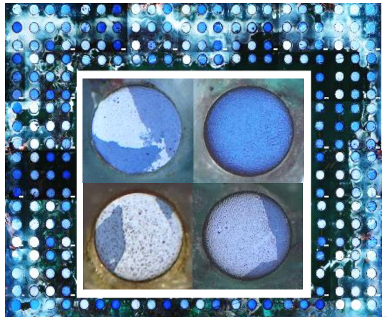
Accelerated Testing
Thermal and mechanical cycling

Failure electrical detection and lifetime analysis

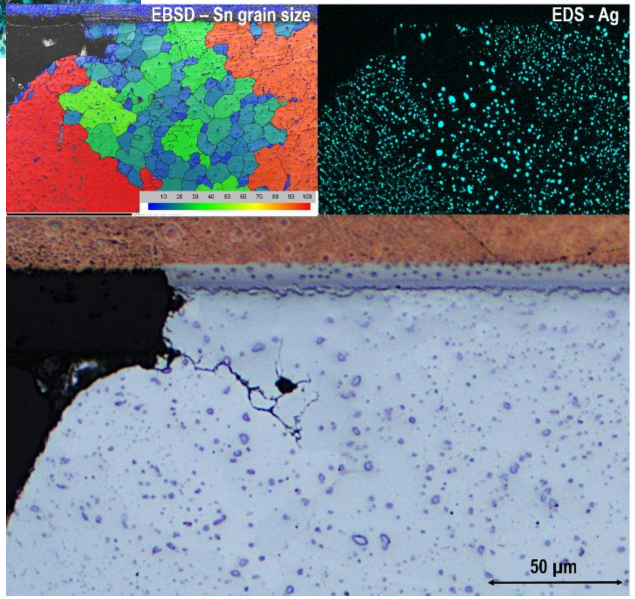
Comparison between different types of components and fatigue tests

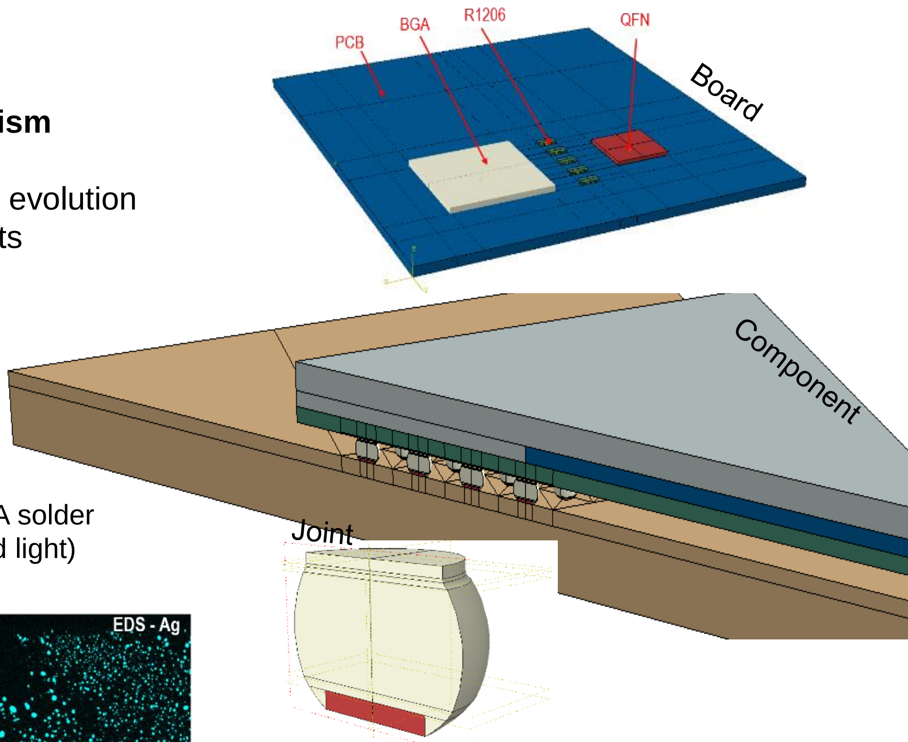
Microstructure investigations
Solder initial state and failure mechanism

Relationship between failure and microstructure evolution
Comparison with failure detection results



Top view of BGA solder balls (polarized light)





Finite element analyses

Location of stresses and strains in solder joints

Correlation with failure results (cross-section, detection)

Taking into account solder anisotropy for more accurate outputs

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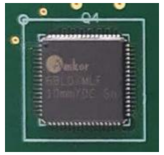
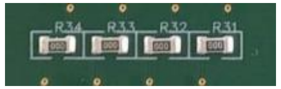
Thermal cycling [-55 ; 125]°C : solder lifetime analysis

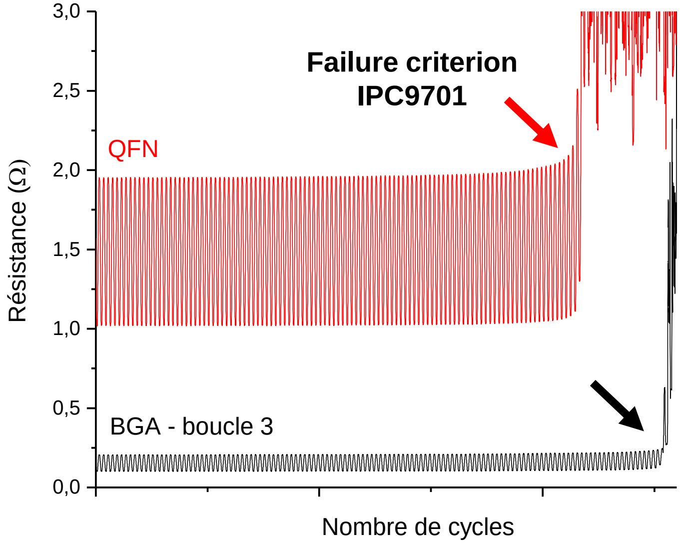


QFN68

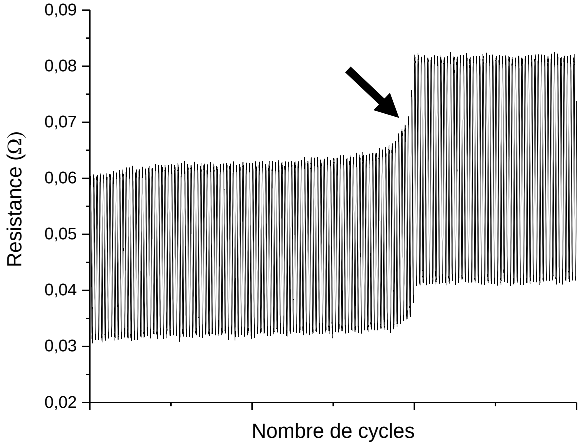
BGA288



R1206

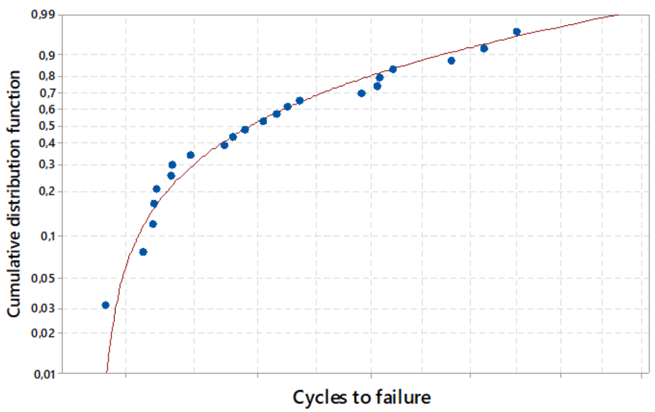


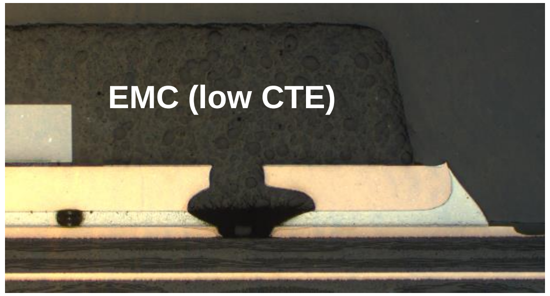
4-wire resistance monitoring
Failure detection



QFN68 - Thermal cycling [-55 ; 125]°C

3-parameter Weibull

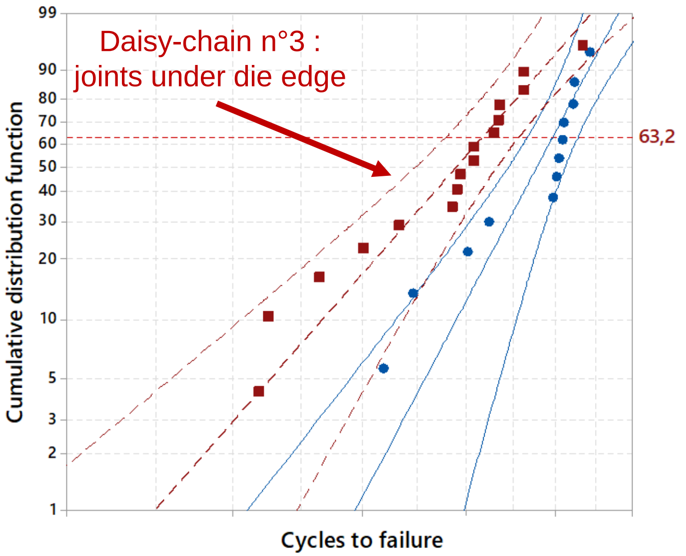


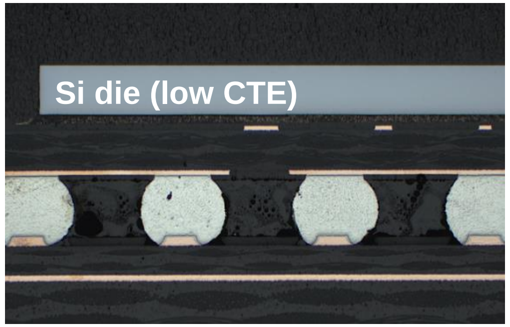


Life data analysis

Impact of CTE of die and epoxy molding compounds

BGA288 - Thermal cycling [-55 ; 125]°C

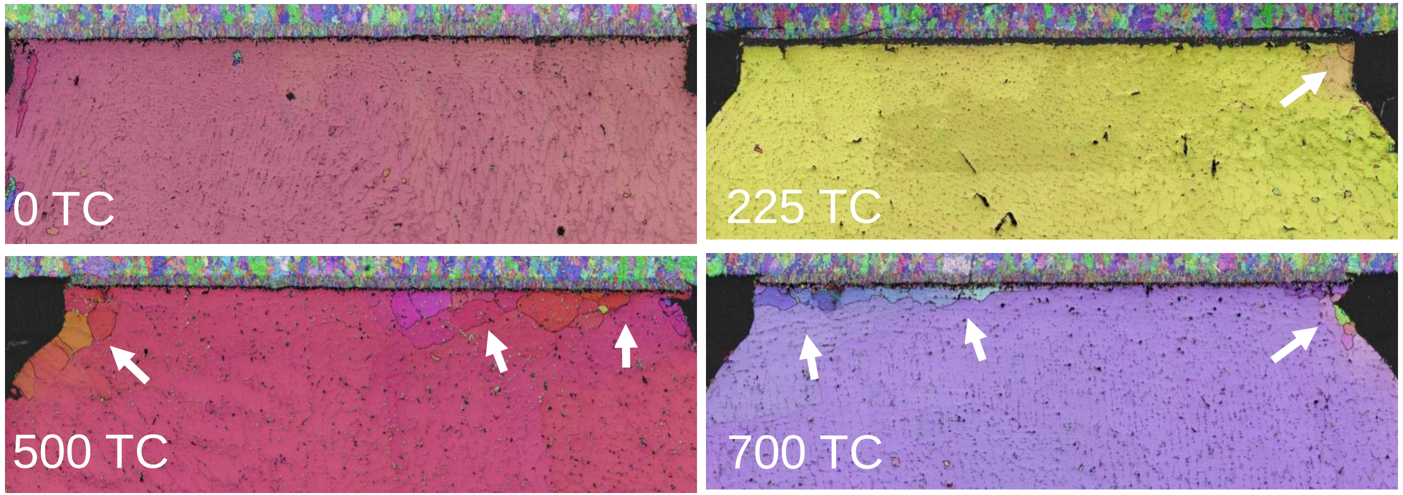




Thermal cycling [-55 ; 125]°C : microstructure investigations

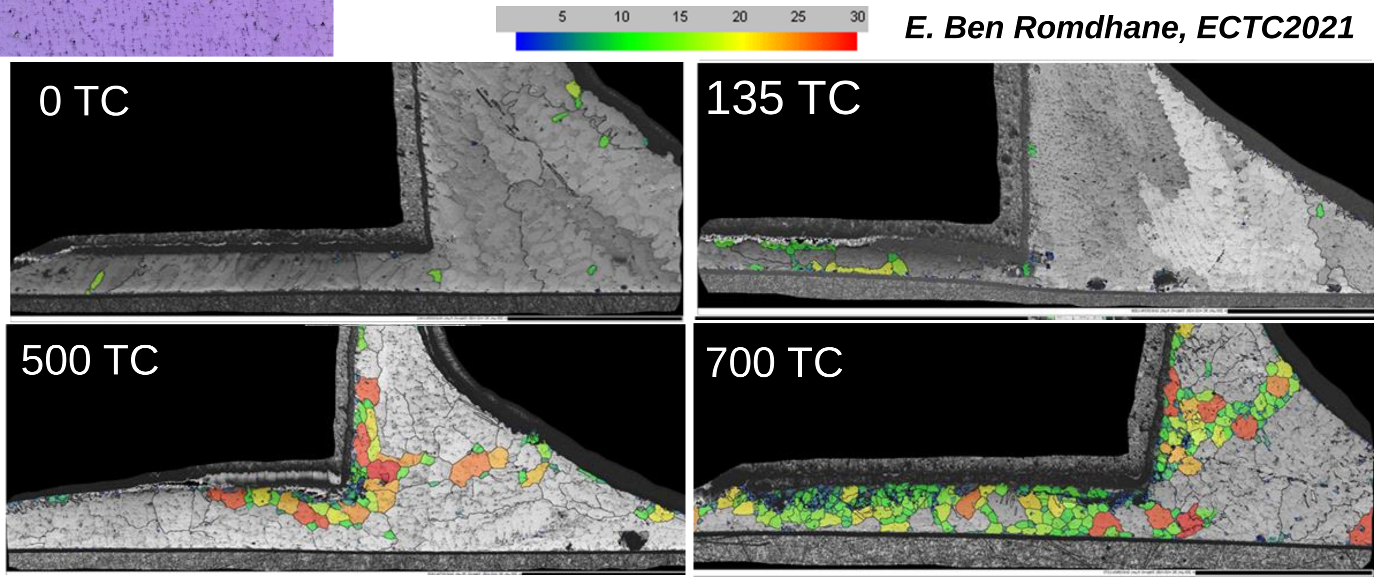
What are the SAC305 solder failure mechanism steps ?
How does the solder microstructure control cracking that leads to failure ?
What is the initial microstructure impact on solder failure ?

E. Ben Romdhane, ESREF2021



Tin grain orientation map

EBSD with



E. Ben Romdhane, ECTC2021

Recrystallization : creation and rotation of new small tin grains in the most stressed regions

Favorable path for intergranular **crack propagation**

Recrystallized tin grain size map

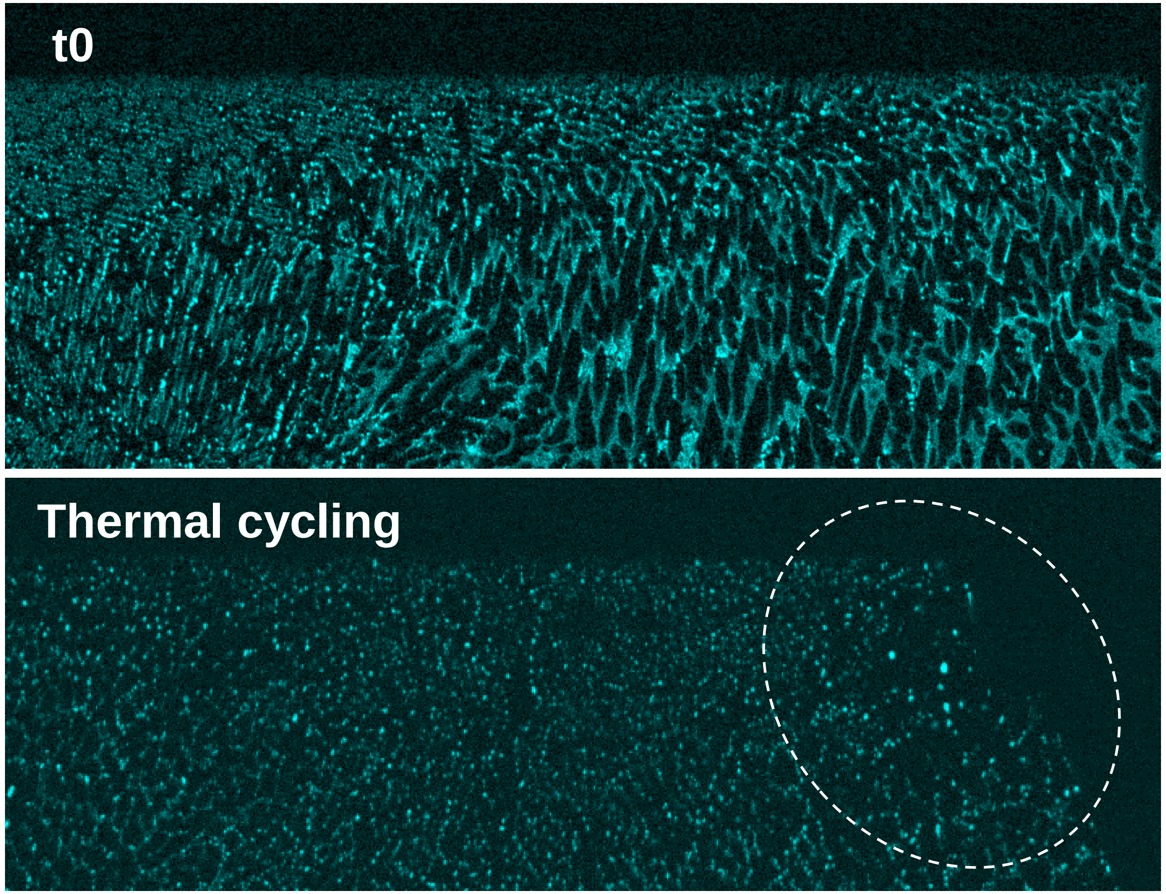
Thermal cycling [-55 ; 125]°C : microstructure investigations

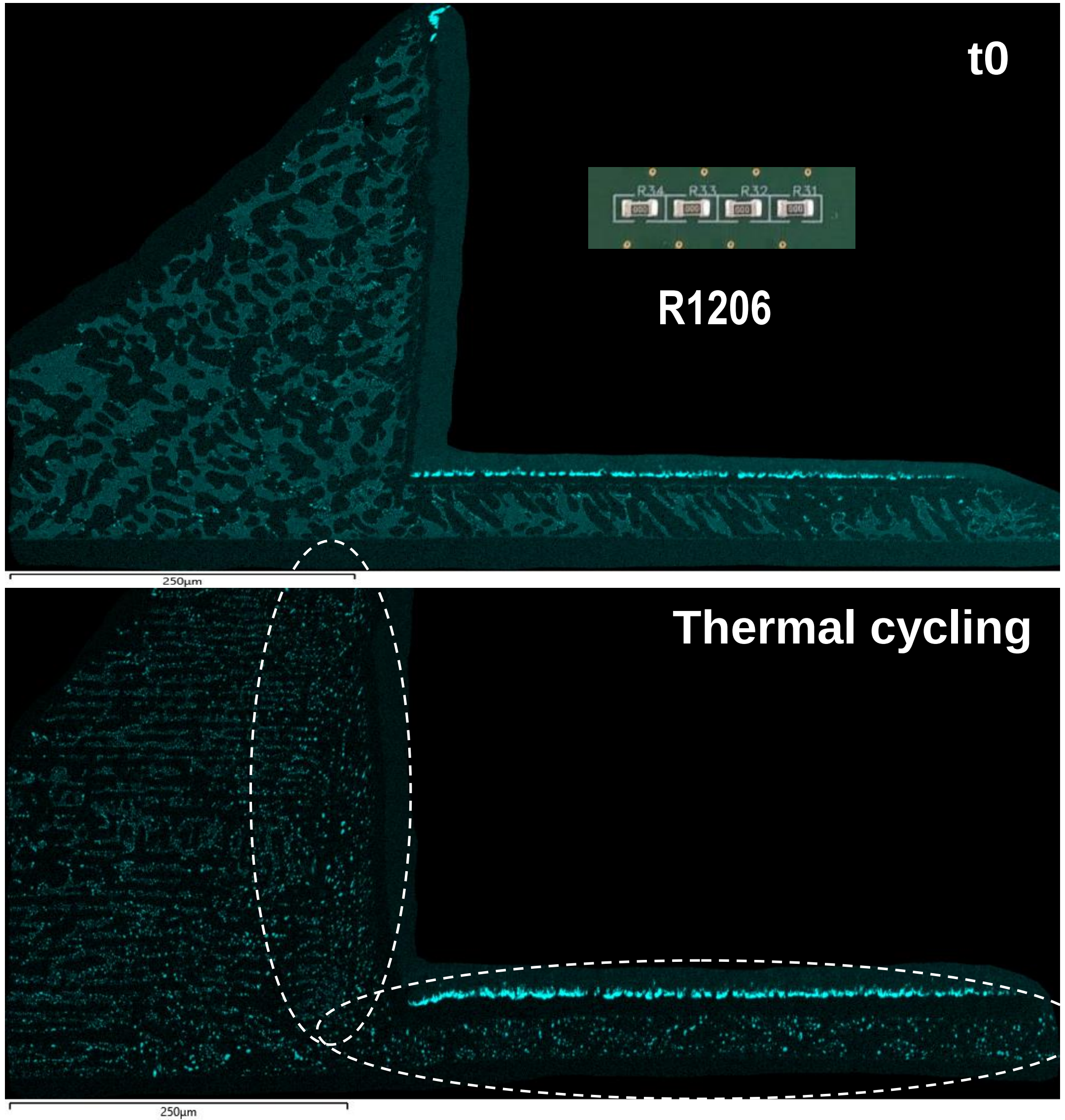
E. Ben Romdhane, ECTC2021

BGA288

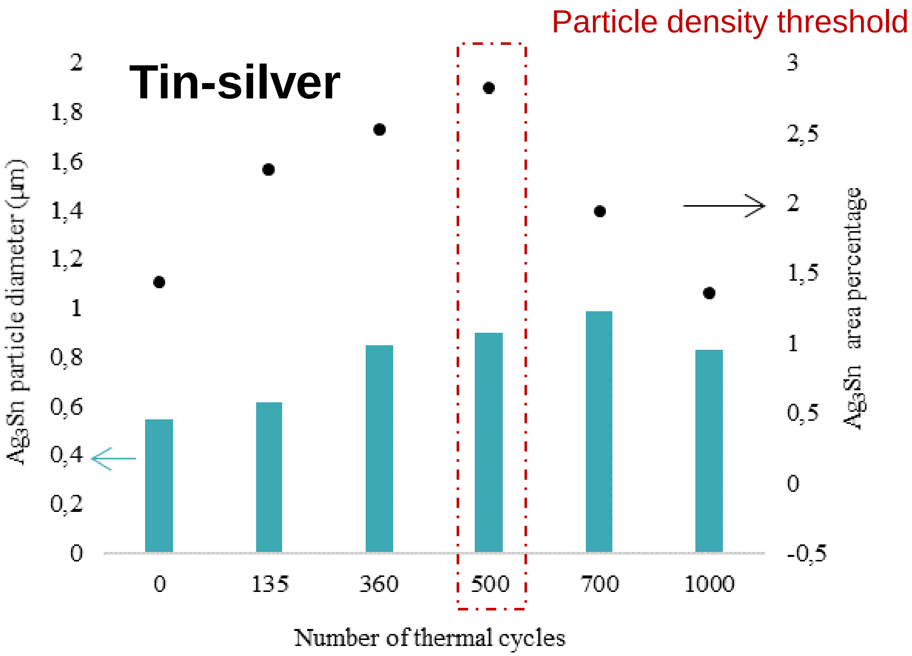
Ag_3Sn precipitate coalescence and loss of dendritic structure in the most stressed regions

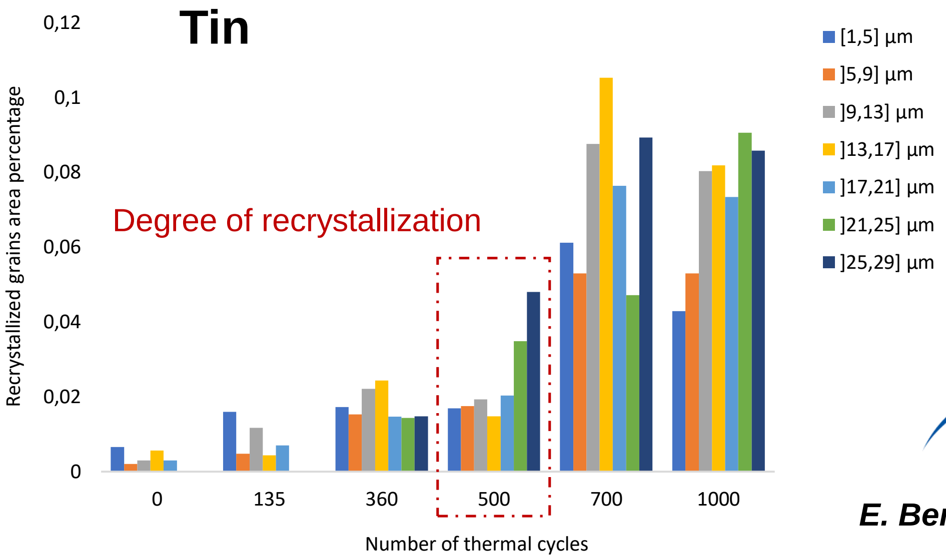
Ag EDS map





Thermal cycling [-55 ; 125]°C : microstructure investigations



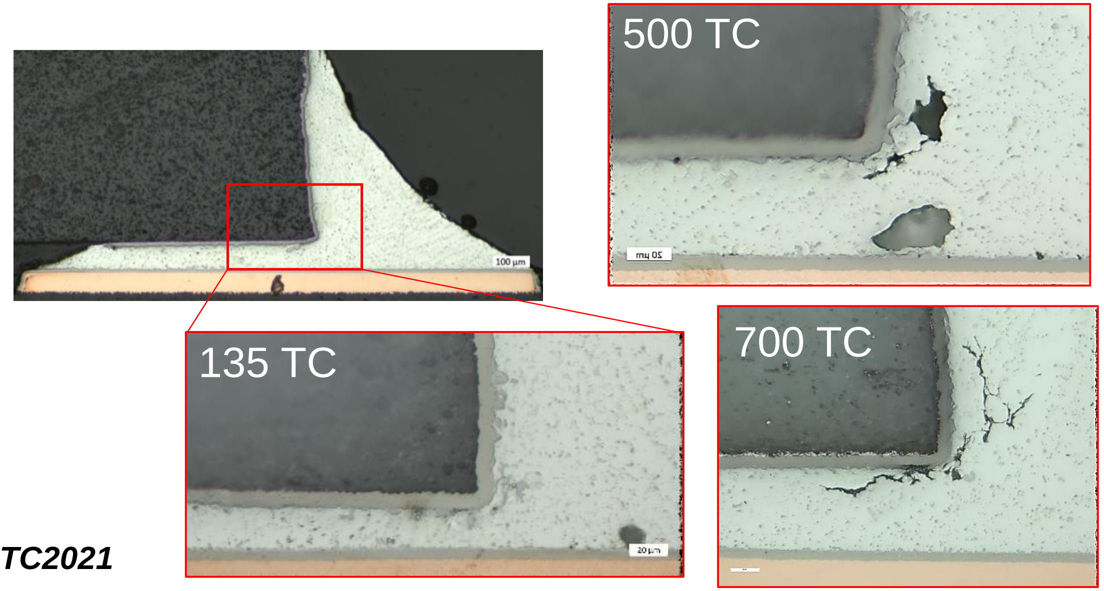


EBSD data → indicators of microstructure degradation

- Ag_3Sn precipitate size
- Tin grain size
- Tin grain boundary angle

Looking for a SAC alloy damage criterion

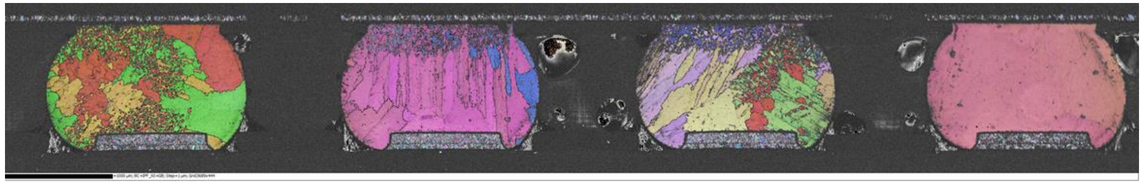
- common to any type of solder joint
- to correlate with crack initiation and propagation
- to correlate with failure detection results
- to use in a microstructure-based fatigue model

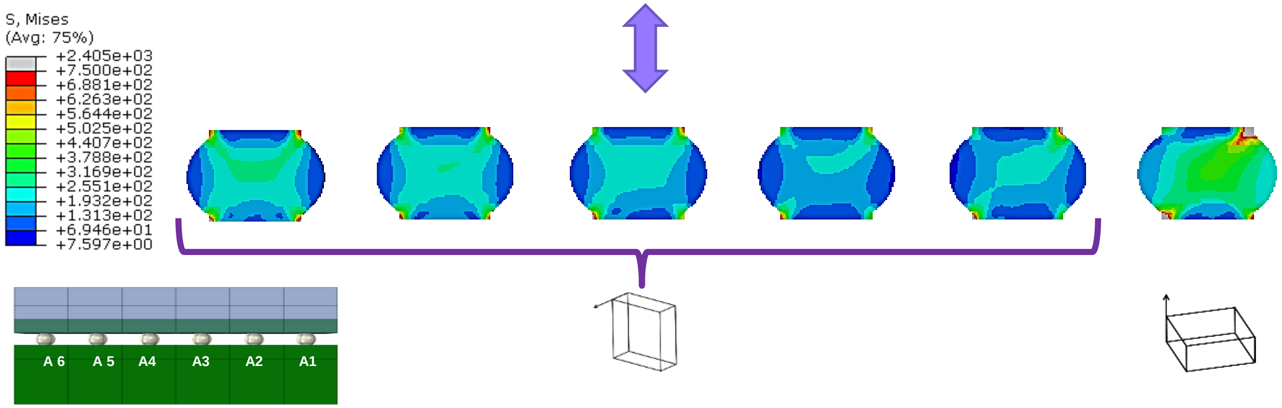


E. Ben Romdhane, ECTC2021

Finite element analyses

EBSD crystal orientation map

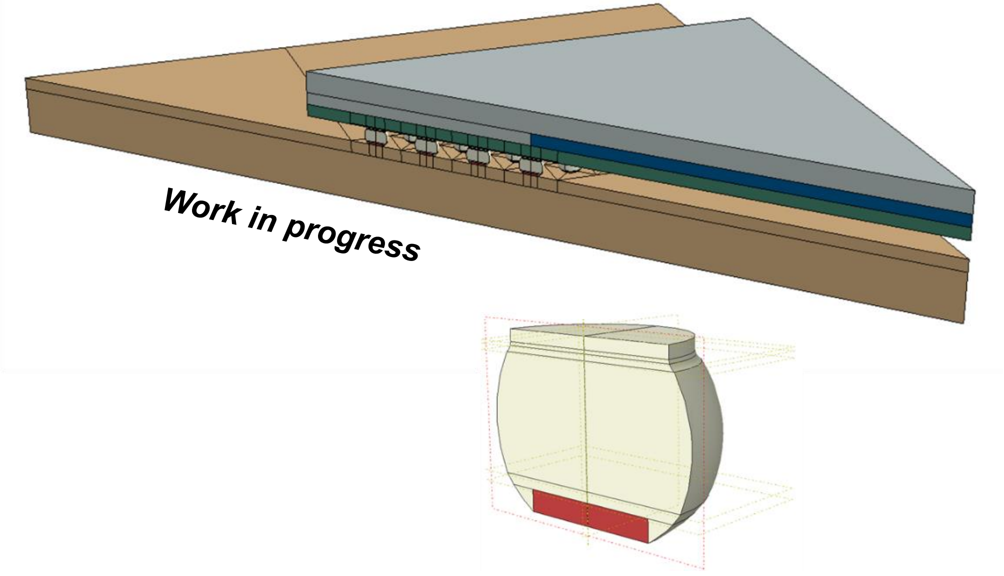




Finite element model of BGA solder joints with different tin crystal orientations

Effect of as-reflowed microstructure on thermomechanical behavior of solder joints

E. Ben Romdhane, ECTC2020



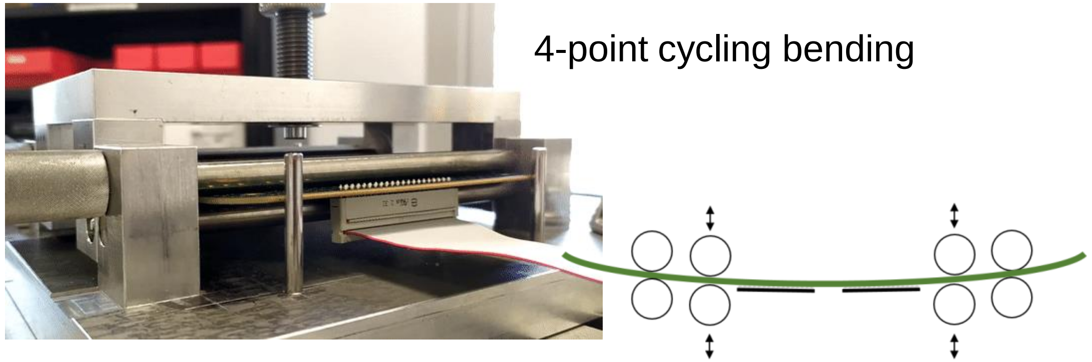
Finite element model a BGA288 component

Correlation with experimental data (location and probability of first failure)

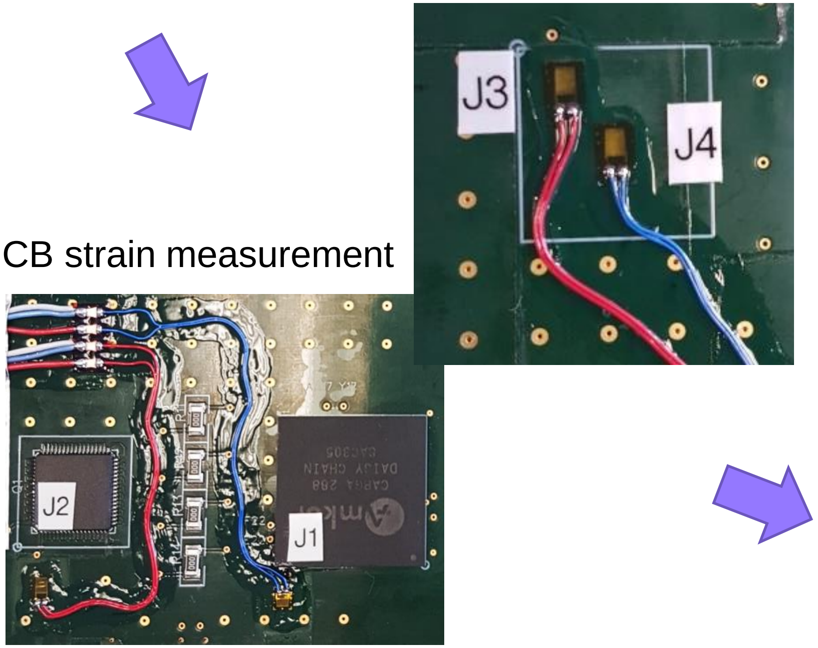
Definition of a fatigue criterion for the modeling of solder damage

Mechanical cycling : alternative to thermal cycling ?

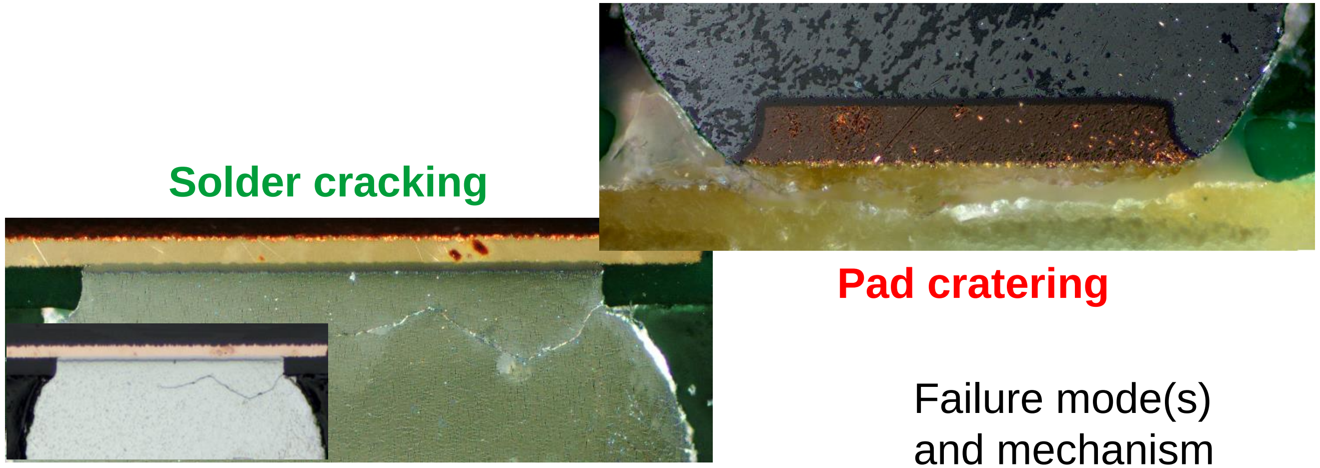
Can we go faster than standard testing ?



4-point cycling bending



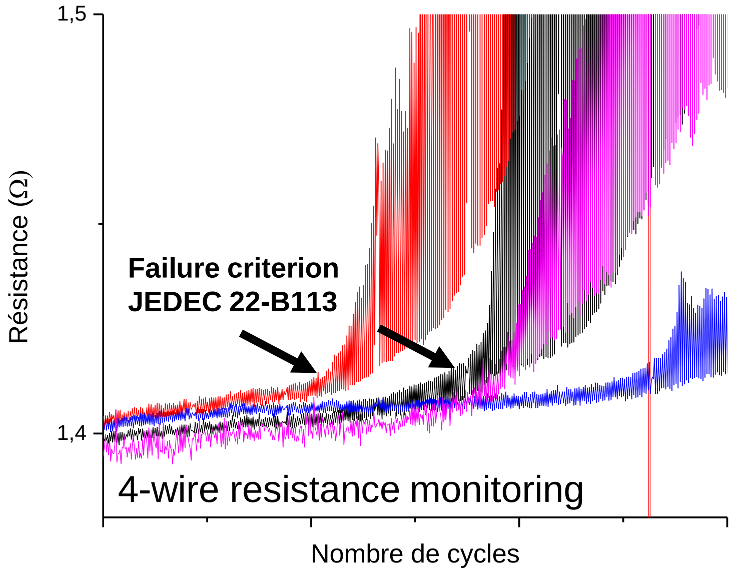
PCB strain measurement



Solder cracking

Pad cratering

Failure mode(s)
and mechanism



4-wire resistance monitoring

Comparison with thermal cycling

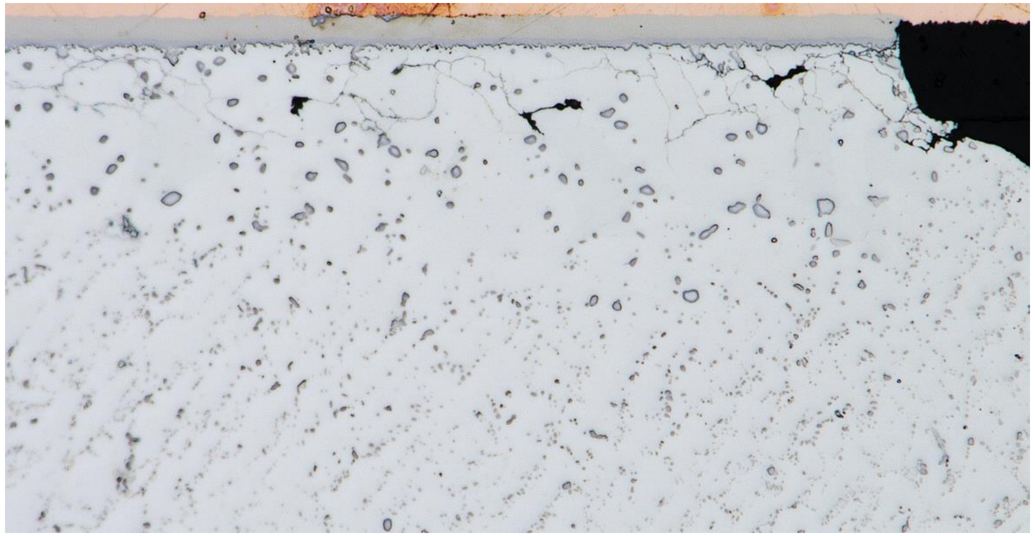
Fatigue lifetimes
Stresses and strains in solder joints and PCB

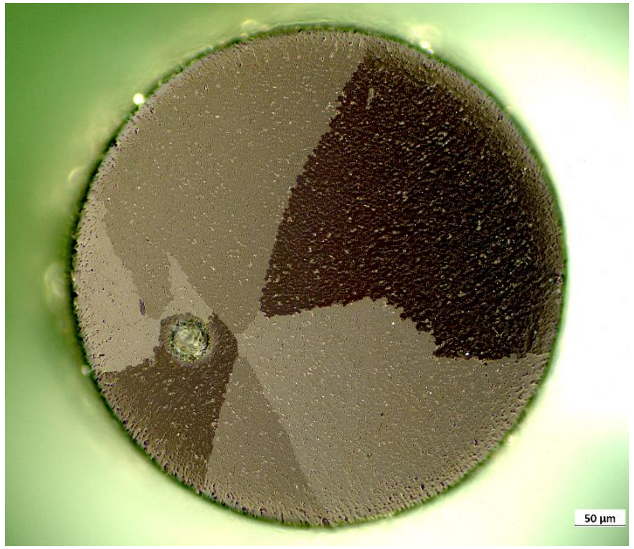
Conclusions

Detailed description of the **SAC solder failure mechanism** (microstructure degradation, crack initiation and propagation)

Comparison between the measured **solder fatigue lifetime** (electrical monitoring) and the **failure mechanism steps**

EBSD data allow the search of a **microstructural criterion** that describes solder damage and failure





Tin anisotropy (grain orientation) is considered in microstructure and failure analyses as well as in **finite element analyses**

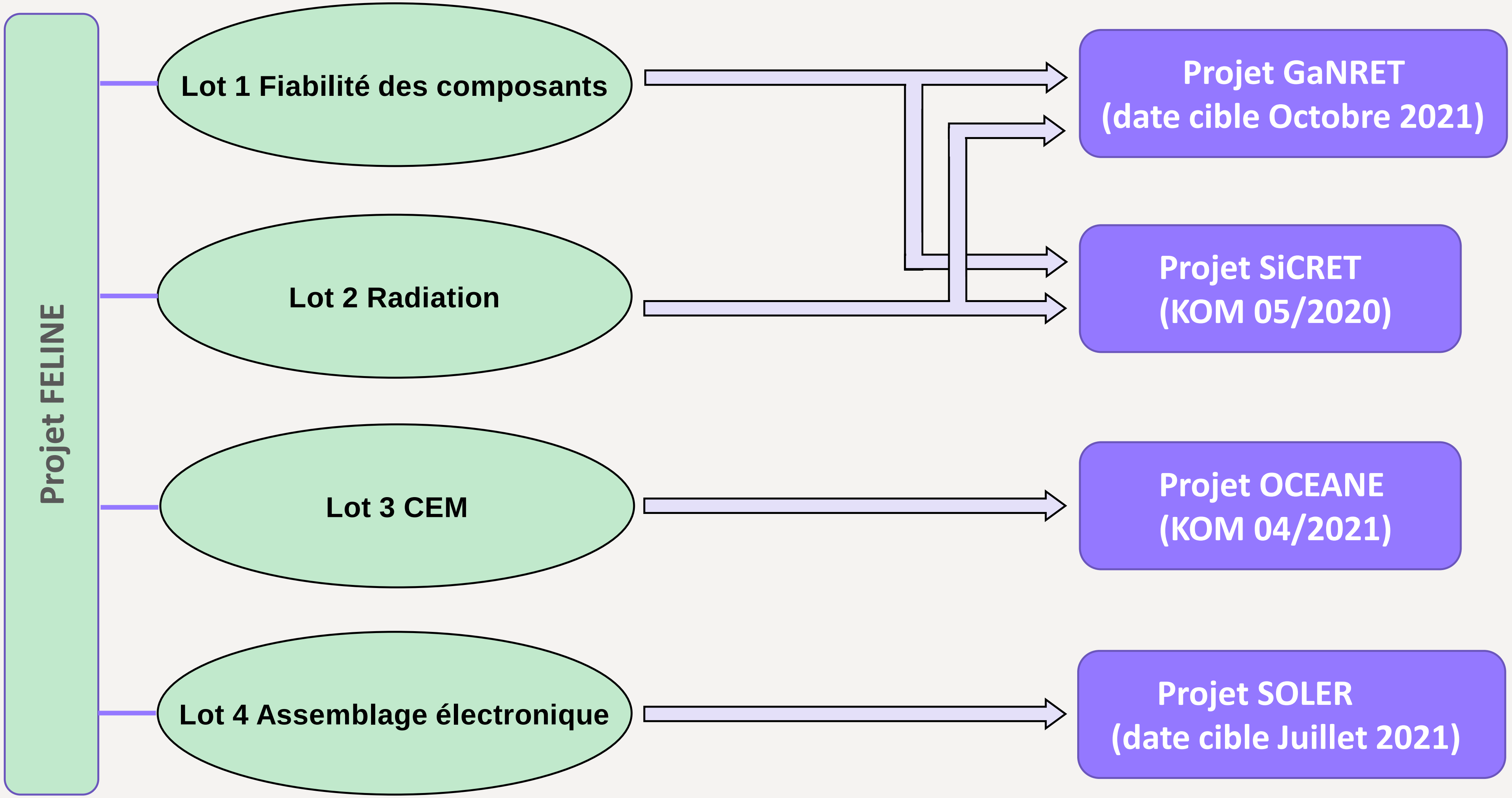
Solder mechanical and thermomechanical fatigue behaviours are compared in order to implement **faster board level testing**

FELINE

Conclusions

What is next…

Après FELINE



Projet FELINE

Lot 1 Fiabilité des composants

Lot 2 Radiation

Lot 3 CEM

Lot 4 Assemblage électronique

Projet GaNRET
(date cible Octobre 2021)

Projet SiCRET
(KOM 05/2020)

Projet OCEANE
(KOM 04/2021)

Projet SOLER
(date cible Juillet 2021)

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LAAS-CNRS, INSA Toulouse, IMS Bordeaux, IETR-CNRS, IES-CNRS

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