



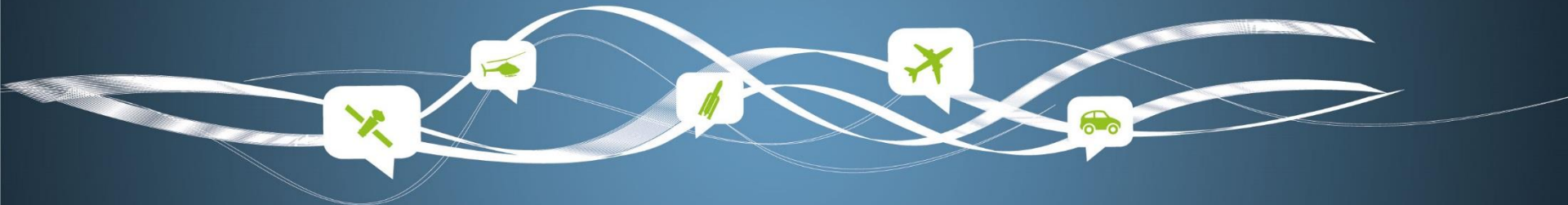
LES RENDEZ-VOUS FIABILITE DU CFF



EPowerDrive Project

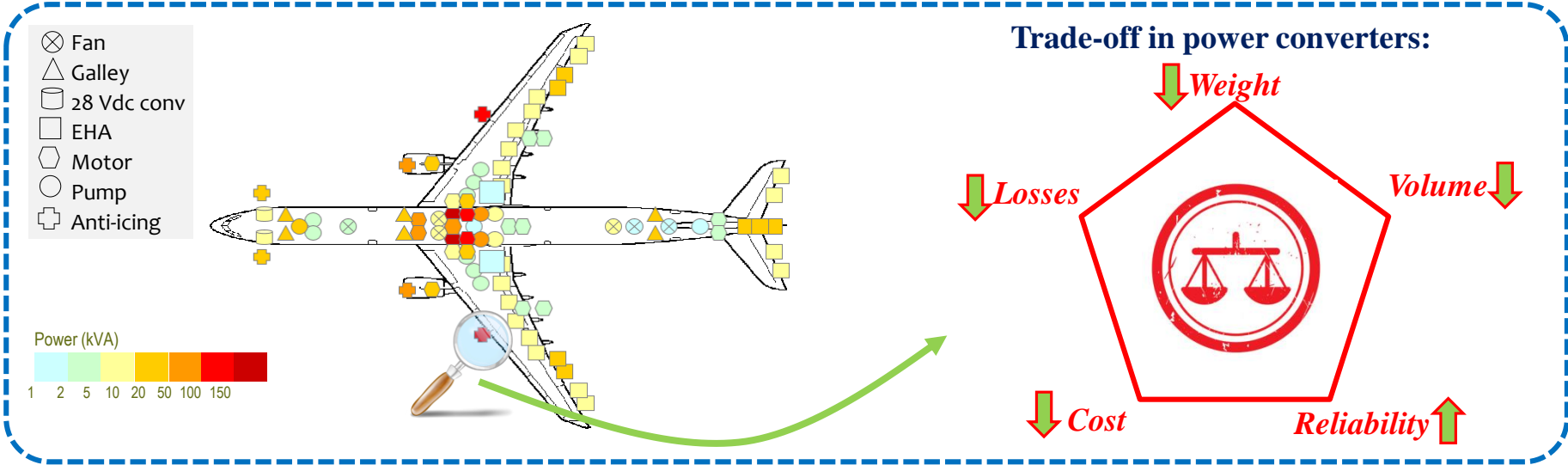
Bernardo Cougo

Senior Expert on Power Electronics

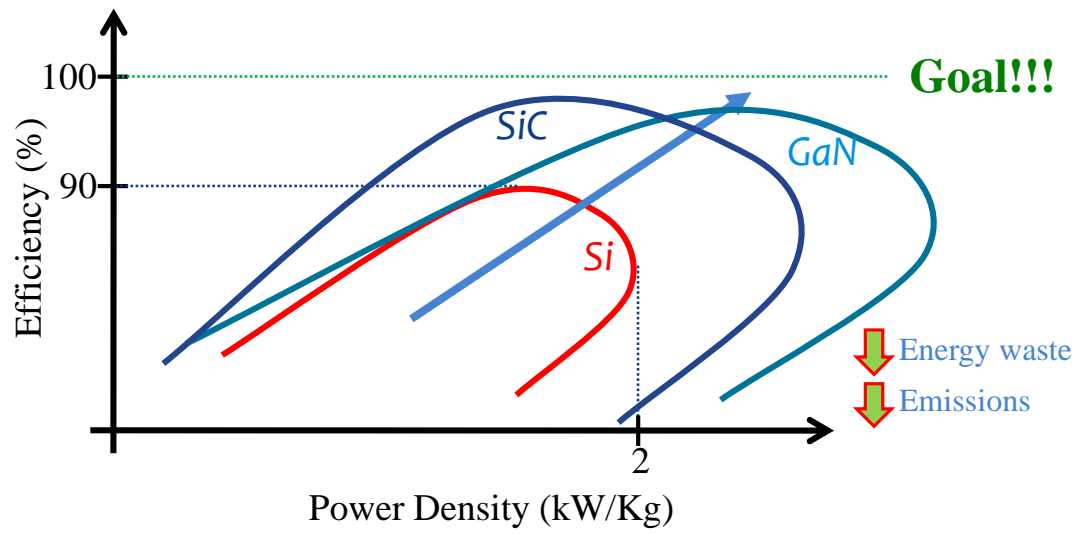
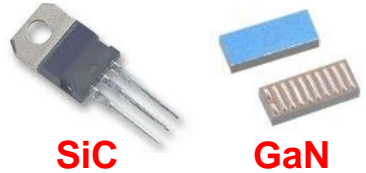


Electrical Applications in Aircrafts

More Electrical Aircraft



Wideband Gap Semiconductors





OBJECTIVES

- Propose technologies, models and tools to increase power density and efficiency of the the whole electromechanical chain using WBG semi-conductors (Silicium Carbide SiC and Gallium Nitride GaN)



8,4 M€



48 months (oct.17 – oct 21)

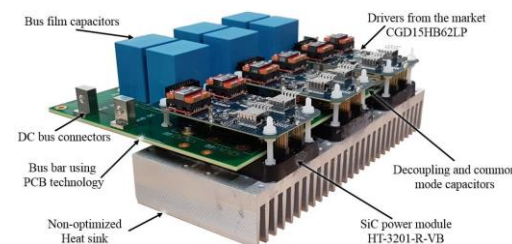
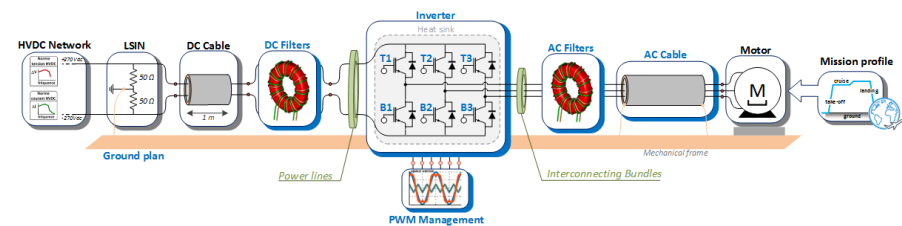


AEROCONSEIL, AIRBUS, APSI 3D, ELVIA PCB, LIEBHERR, NIDEC/LEROY SOMER, SAFRAN, (TFE ELECTRONICS), ZODIAC, LAPLACE, SATIE, G2ELAB

Key Results

- WP1 (Optimisation)** → Tools for Multi-Disciplinary Optimisation
- WP2 (EMC)** → HF models for optimized filter design
- WP3 (Power Electronics)** → Technologies for high-power density, high efficiency inverter
- WP4 (Electric Motors)** → Models for better understanding of iron losses, potential of additive manufacturing

2 Demonstrators (1 based on SiC, 1 based on GaN)



6 patents



3 PhDs



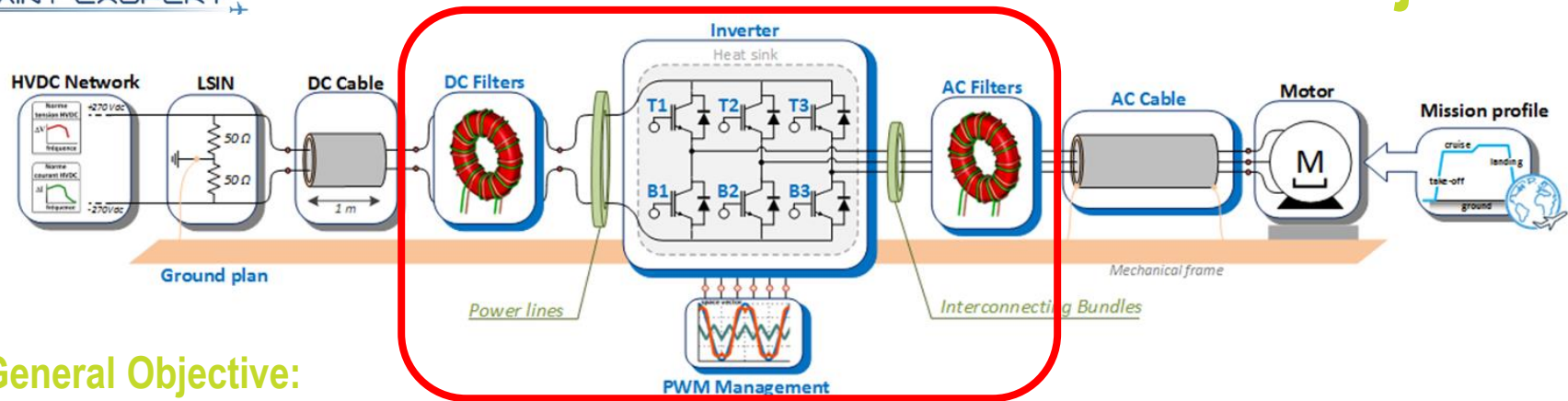
15 publication



10 partners



22 people



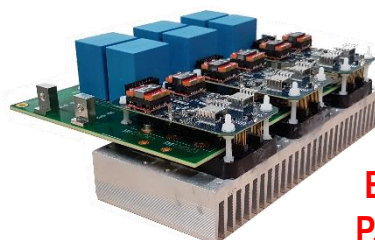
General Objective:

- ❑ Contribute with models, characterization results and technologies in order to help optimizing the Power Drive System

Specific Objective:

- ❑ Design, Built and Test a Full Compliant **70kVA/56kW/540V** THREE-PHASE INVERTER

SiC-Based



- Simple Topology, reliable and performing components, optimized efficiency and filters

Power Core
Efficiency = 99%
P. Dens. = 15kW/kg

Reference Filter
Efficiency = 99.2%
P. Dens. = 5.3kW/kg

GaN multilevel



Pilawa Research Group

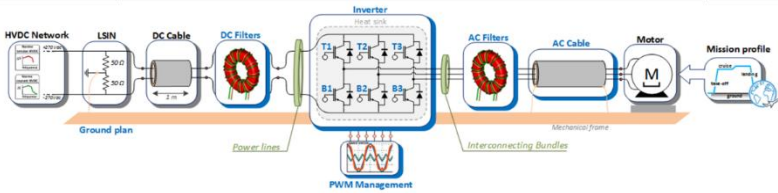
- Performing Topology, components and technology for maximum integration

Power Core + Filters
Efficiency = 98.5%
P. Dens. = 8kW/kg

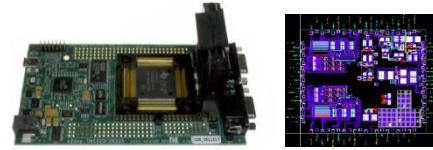
Research Topics on EPowerDrive



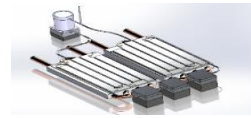
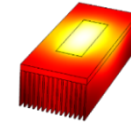
Integrated design by optimization of electrical systems & IRT Positioning



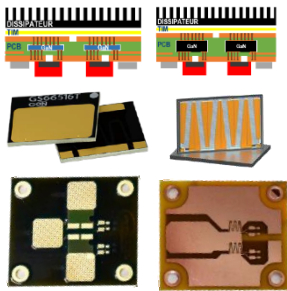
Multidisciplinary design optimization of electrical system



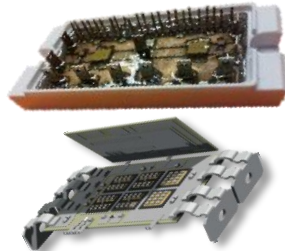
Control card & algorithm, optimized PWM, active gate driver



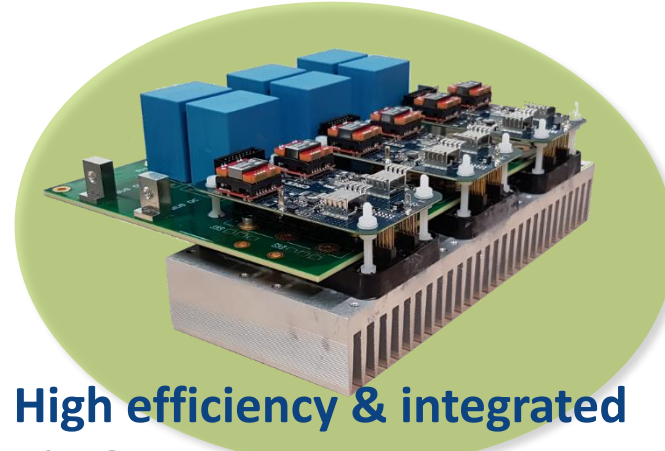
Cooling system optimization



GaN PCB embedded



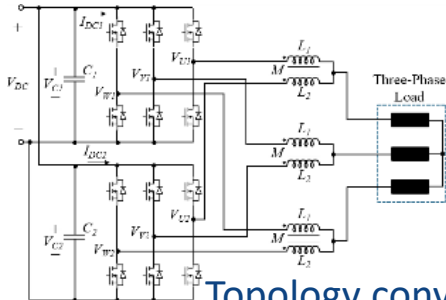
Innovative SiC power module



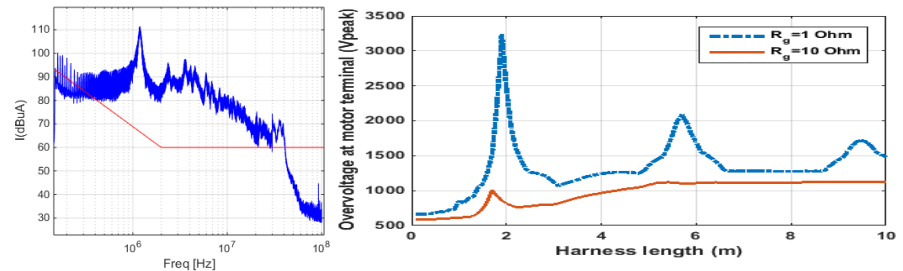
High efficiency & integrated SiC & GaN Power Converter



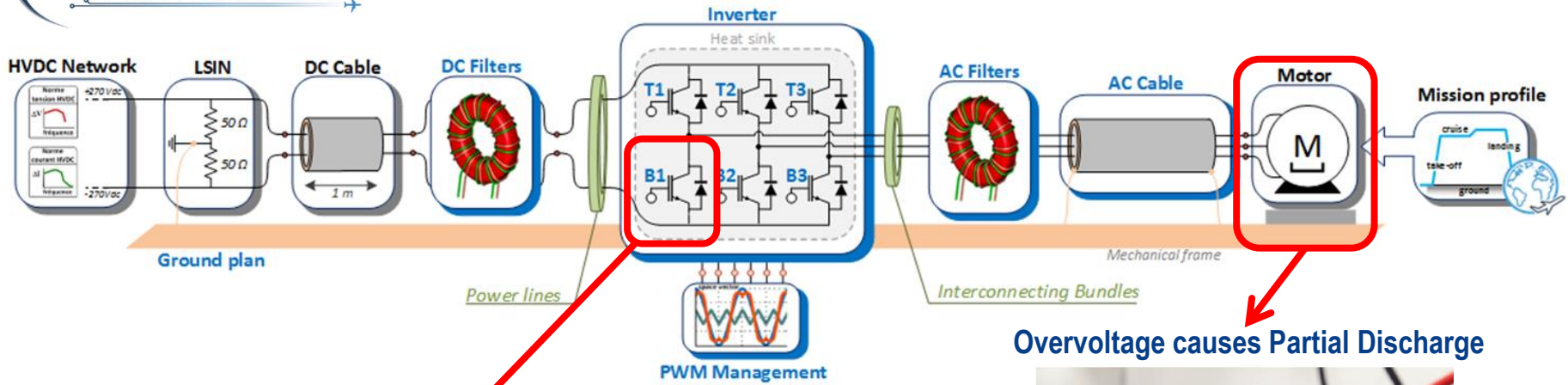
Component, power module & magnetics loss characterization



Topology converter

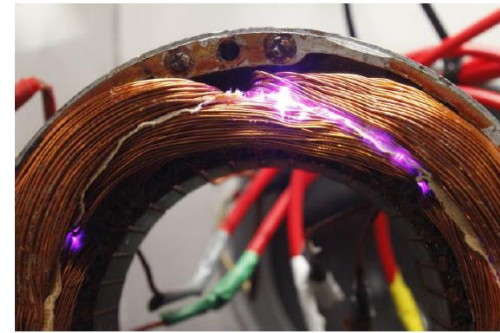


EMI, overvoltage & partial discharge impact evaluation 5

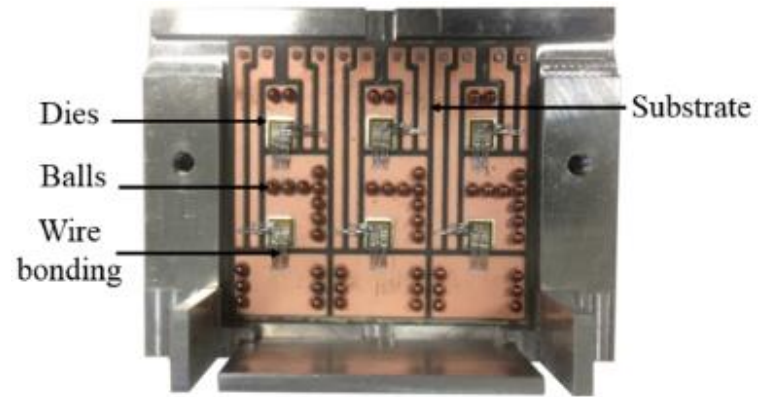
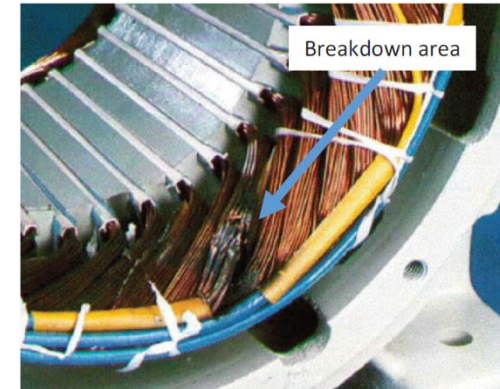


Overvoltage causes Partial Discharge

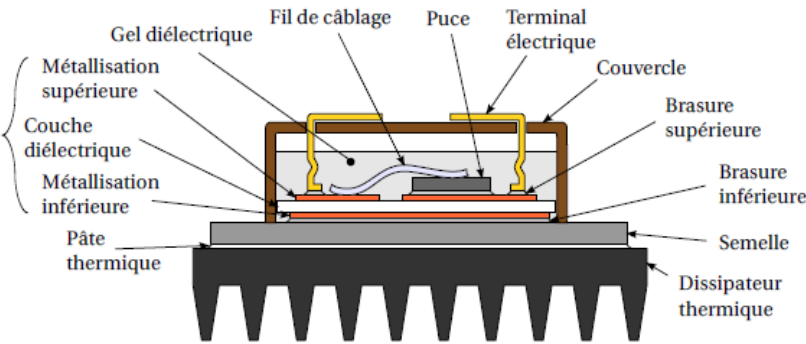
Overvoltage and temperature causes power module failure



Partial Discharge causes motor failure

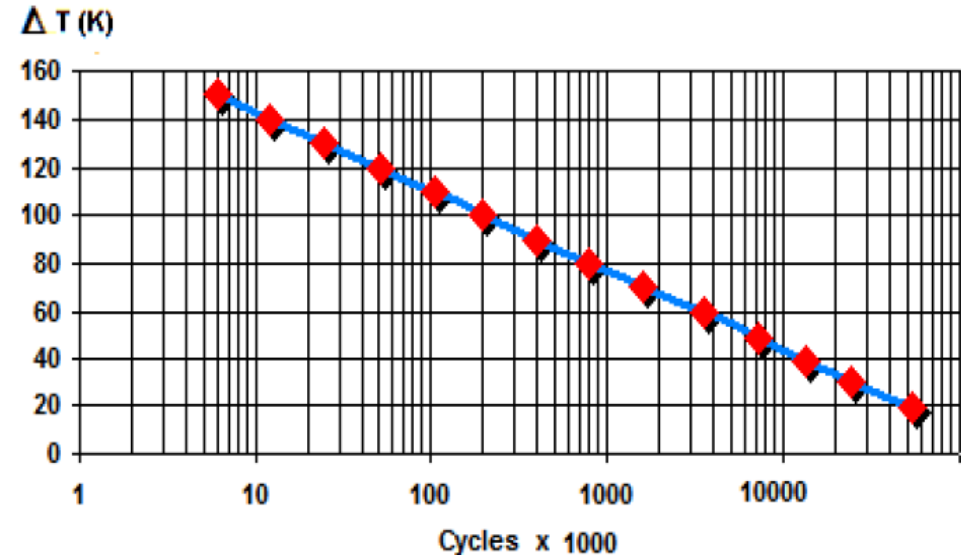


Power Module



Internal structure of a generic power module [1]

Reliability of a power module



Number of cycles to failure versus temperature variation of MOSFET dies inside a power module for automotive applications [2]

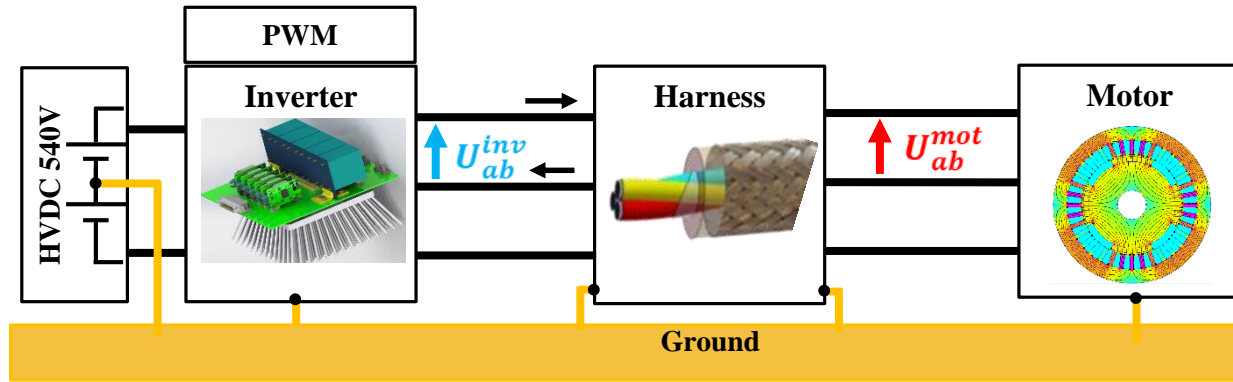
- Small SiC dies = thermal impedance smaller than that of Si.
- Thermal cycles at fundamental frequency can be significant.
- Fast SiC switching induce higher overvoltage at drain-source and gate-source terminals, which may reduce component lifetime.

[1] B. Mouawad, "Assemblages innovants en électronique de puissance utilisant la technique de « spark plasma sintering »,» Ph.D. dissertation, Institut National des Sciences Appliquées de Lyon, 2013

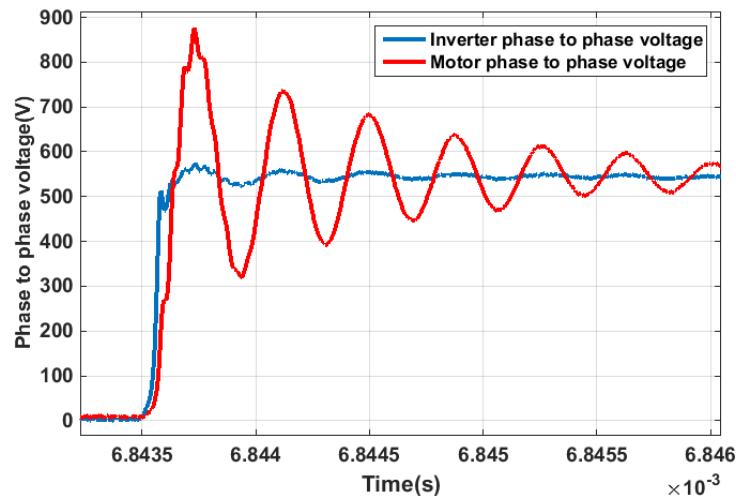
[2] A. Testa, S. De Caro, S. Panarello, S. Patane, "Stress Analysis and Lifetime Estimation on Power MOSFETs for Automotive ABS Systems" IEEE PESC 2008,

Partial Discharge and Overvoltage

- Phase to phase overvoltage in electromechanical chain : inverter + harness + motor



- Example of measured overvoltage on AC motor + 2m harness fed by IGBT inverter (IRT platform)

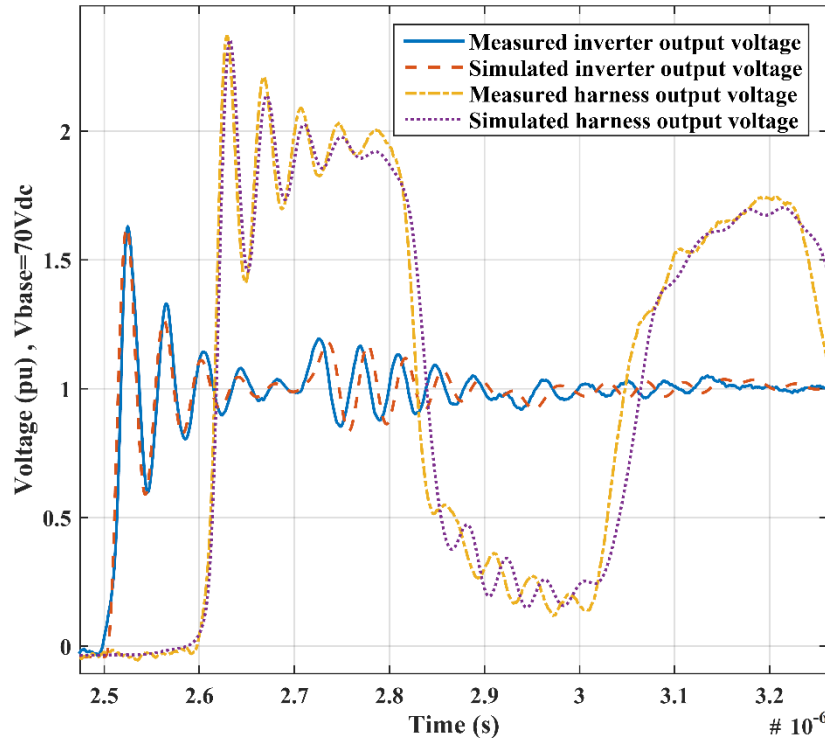


→ Propagation and reflection phenomena along the harness, even for small lengths, cause voltage overshoots across the motor phases

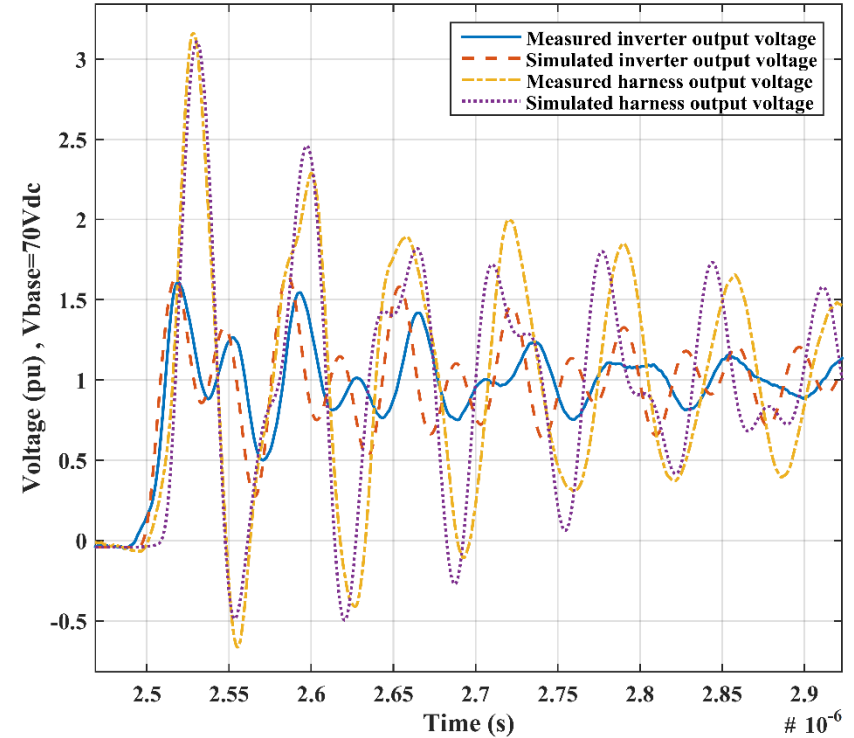
Experimental Investigation

Overvoltage caused by SiC inverter fed a short CF-AWG18 harness having...

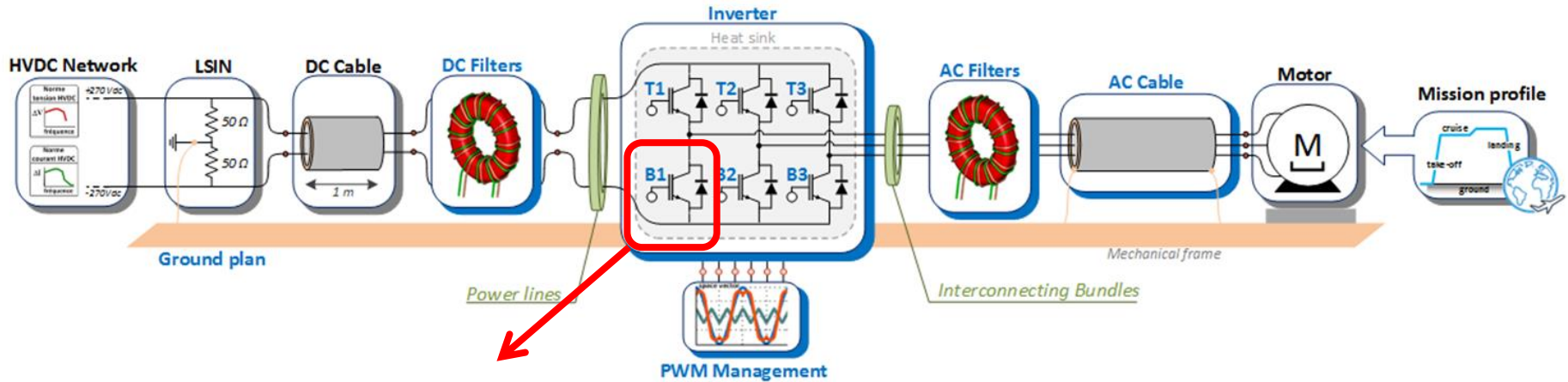
Length of 18.7 m



Length of 2.3 m



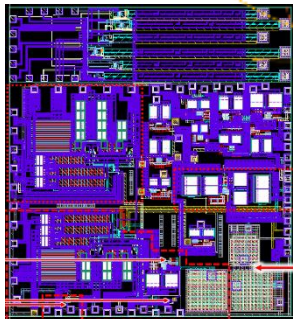
- Very high overvoltage can appear on cables end if its length has a characteristic frequency close to the ringing frequency at the output of the converter
- Simulation with our developed frequency models is fast (**Calculation time < 200ms**) and matches very well experimentation (**Accuracy < 6%**)



Improving reliability of Power Drive System

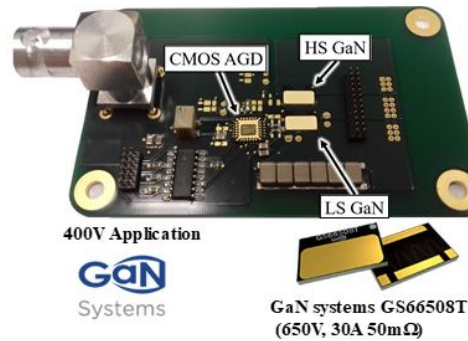
- Reduce Overtoltage
- Reduce Switching Speed
- Reduce Maximum Temperature
- Reduce Thermal Cycles

Active Gate Driver (AGD)

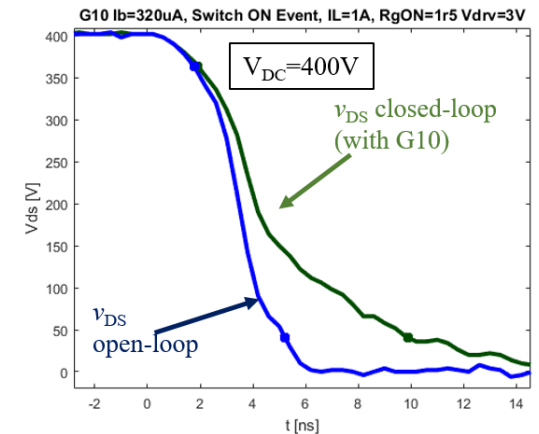


Laplace

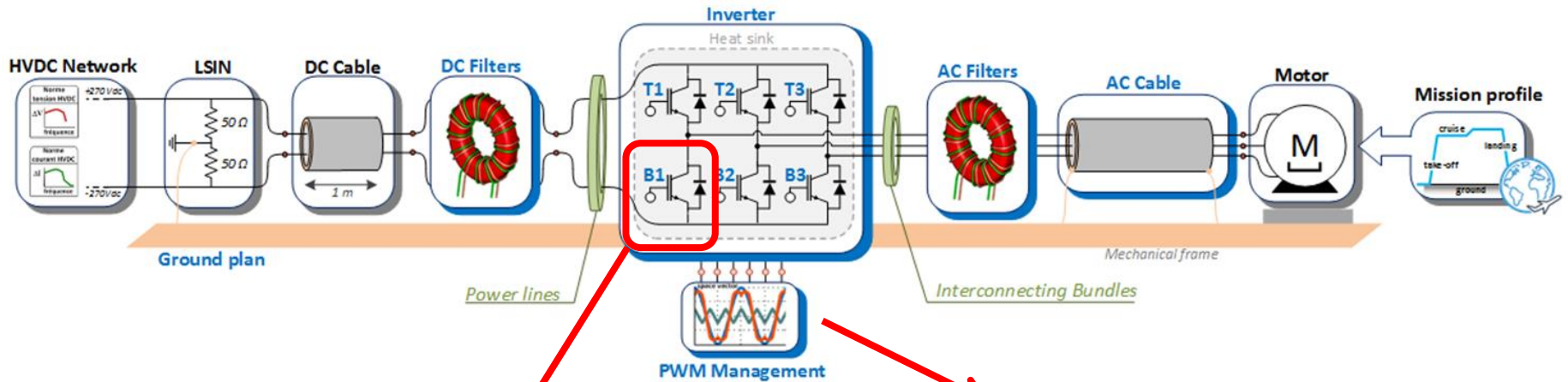
Implementation of AGD



Experimental Results



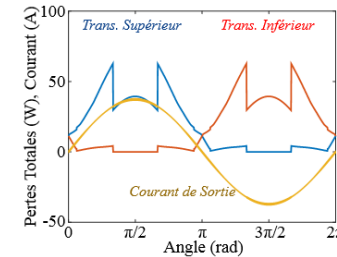
Developed AGD reduce switching speed, overvoltage with small increase on switching losses



Improving reliability of Power Drive System

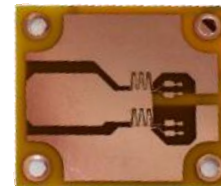
- Reduce Overvoltage
- Reduce Switching Speed
- Reduce Maximum Temperature
- Reduce Thermal Cycles

Control Methods (PWM)



Optimal PWM method to reduce losses and thermal cycles

Packaging and Integration



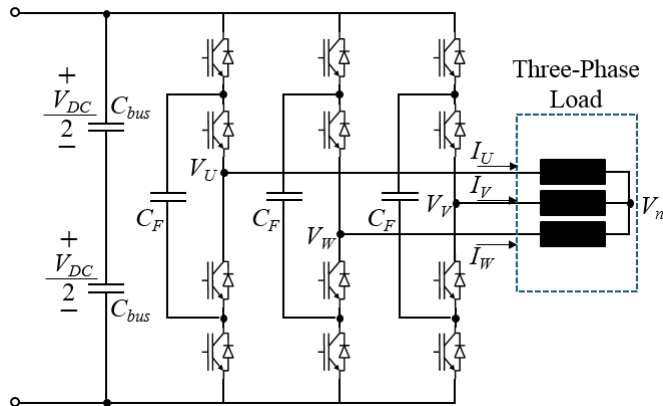
GaN inside PCB



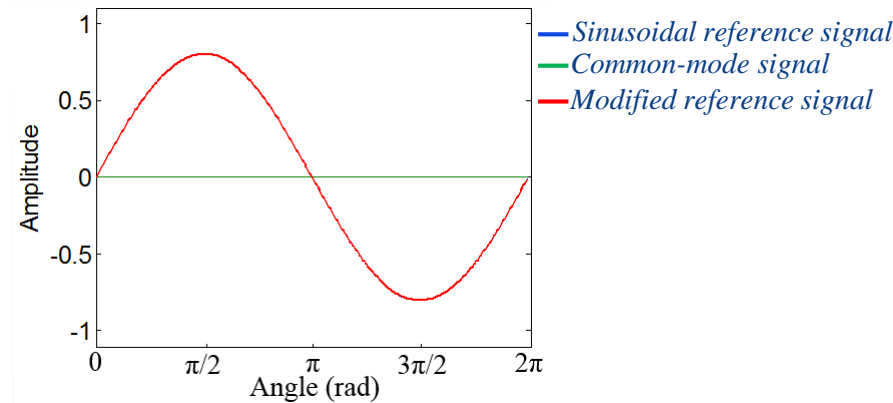
Innovative SiC power module

PWM Methods (Common mode offset)

Floating Neutral Point Configuration

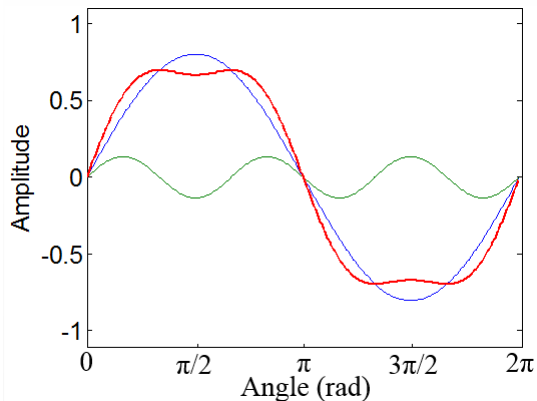


SPWM



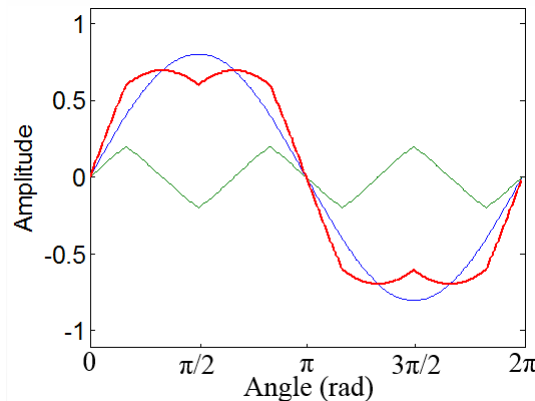
Continuous PWM Methods

THIPWM1/6



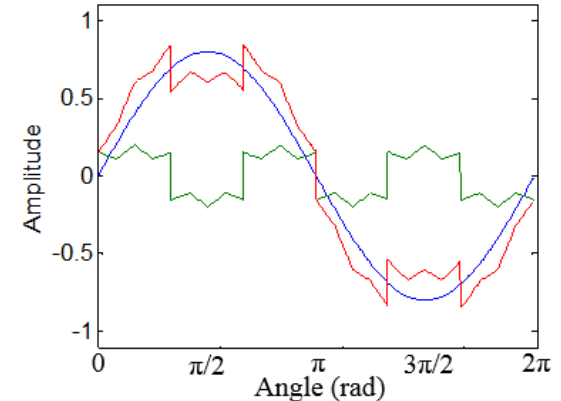
Increase output voltage range

SVPWM



Reduce output voltage harmonics

SV3PWM

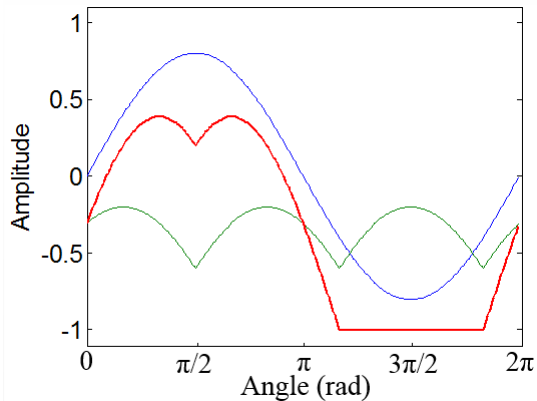


Reduce output voltage harmonics for 3-level conv.

PWM Methods (Common mode offset)

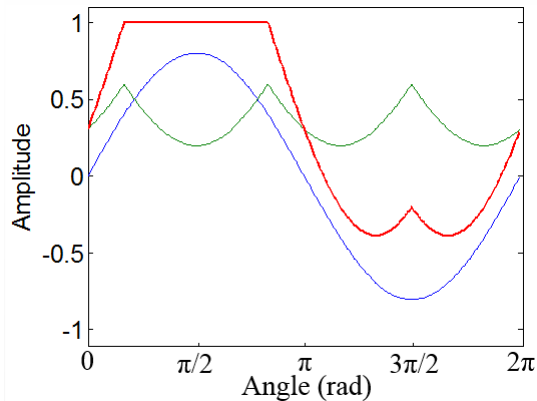
Discrete PWM Methods

DPWMMIN



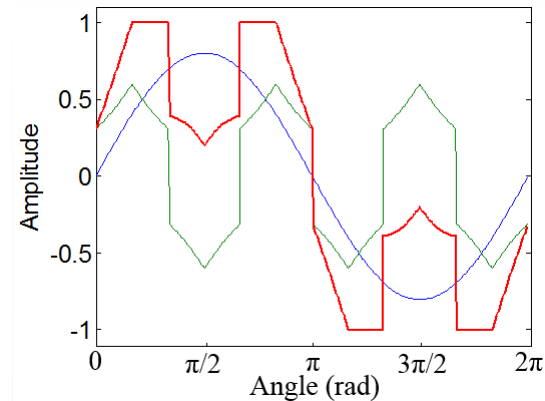
Reduce SW losses
of low-side switches

DPWMMAX



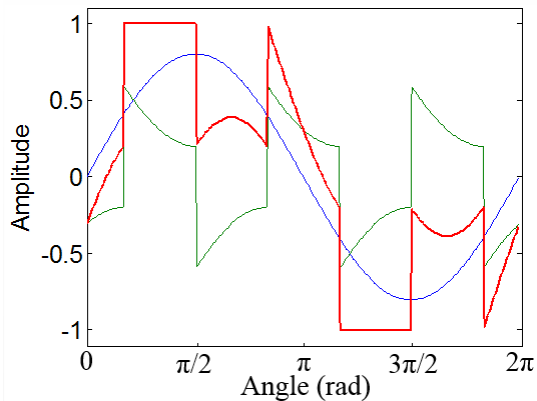
Reduce SW losses of
high-side switches

DPWM3



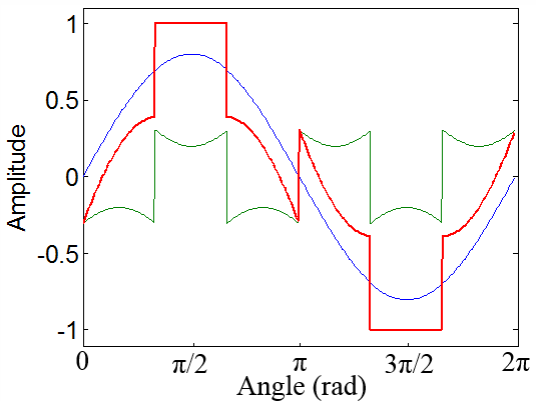
Reduce SW losses for
non-sinus current

DPWM0



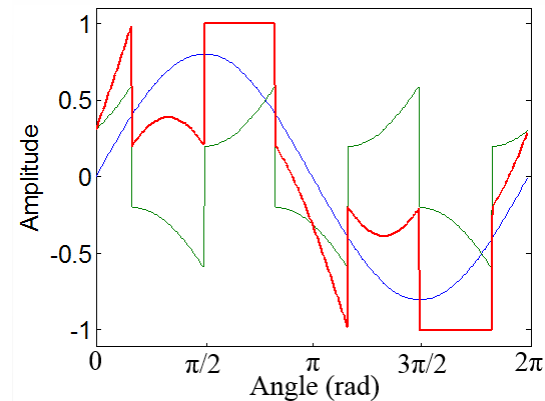
Reduce SW losses
for capacitive load

DPWM1



Reduce SW losses
for resistive load

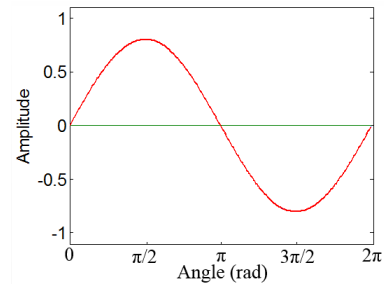
DPWM2



Reduce SW losses for
inductive load

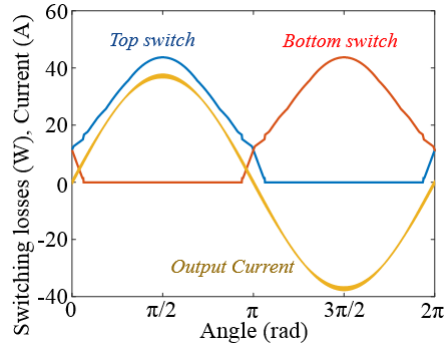
Influence on Losses (2-Level Converter)

SPWM

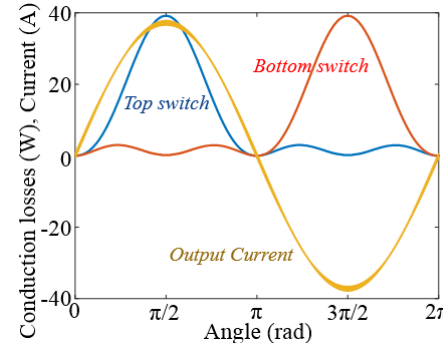


Losses = 152W

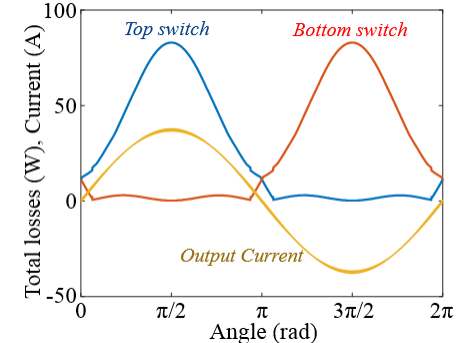
Avg Switching Losses



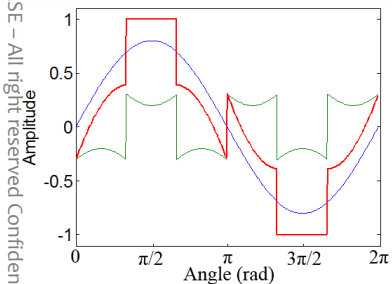
Avg Conduction Losses



Total Transistor Losses

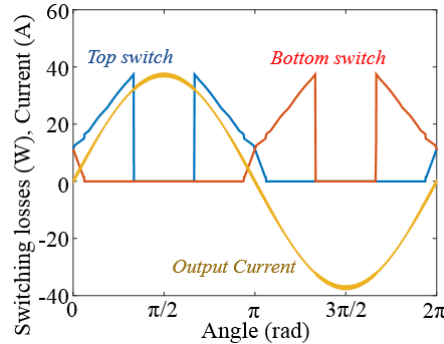


DPWM1

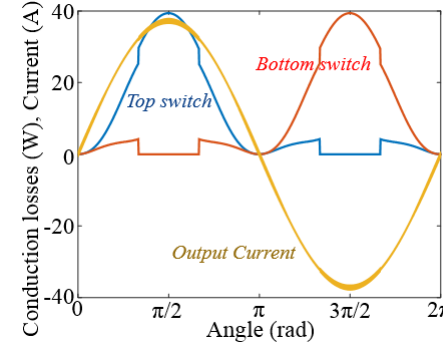


Losses = 110W

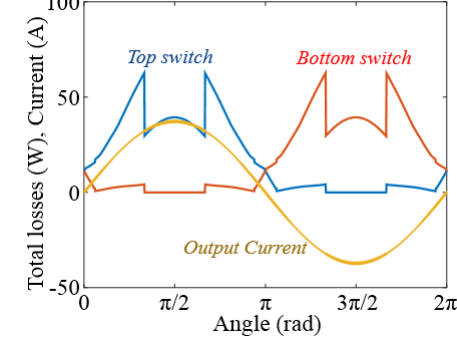
Avg Switching Losses



Avg Conduction Losses



Total Transistor Losses

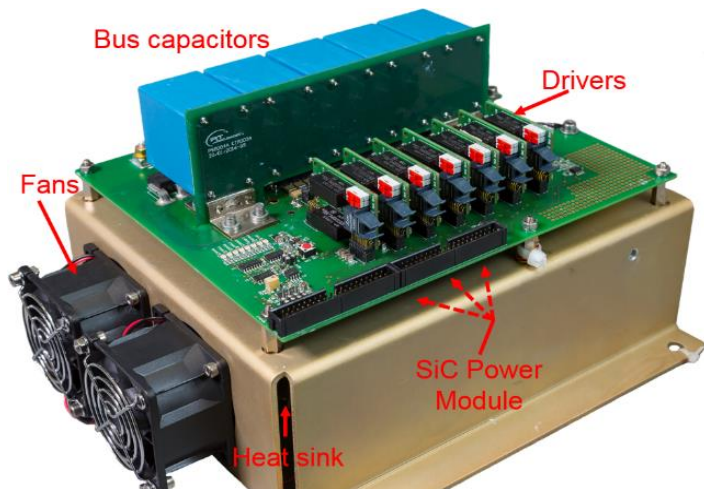


Total losses decrease 28% at 50kHz using a more “adequate” PWM method

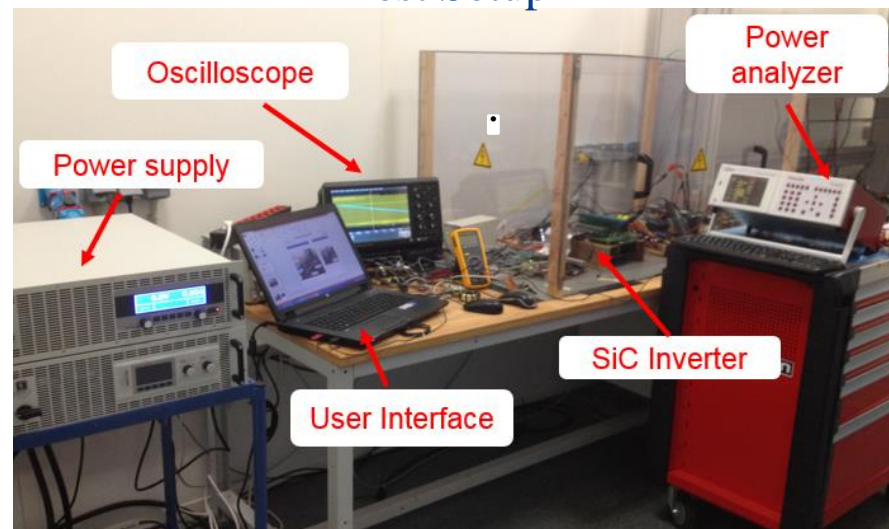
PWM Methods (Experimental Results)

Three-phase SiC Inverter (15kW/540V)

Three-Phase Prototype

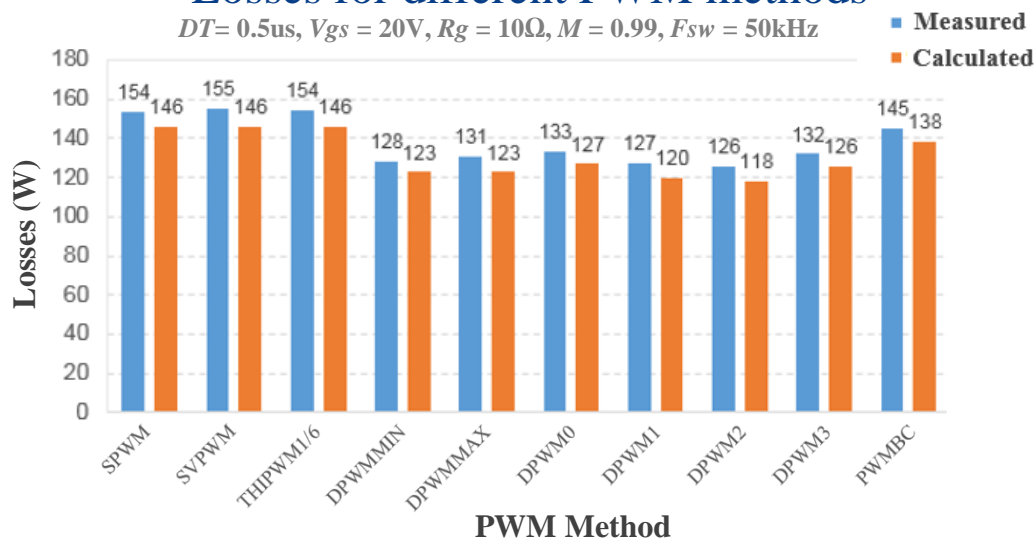


Test Setup



Losses for different PWM methods

$DT = 0.5\mu s$, $V_{gs} = 20V$, $R_g = 10\Omega$, $M = 0.99$, $F_{sw} = 50kHz$

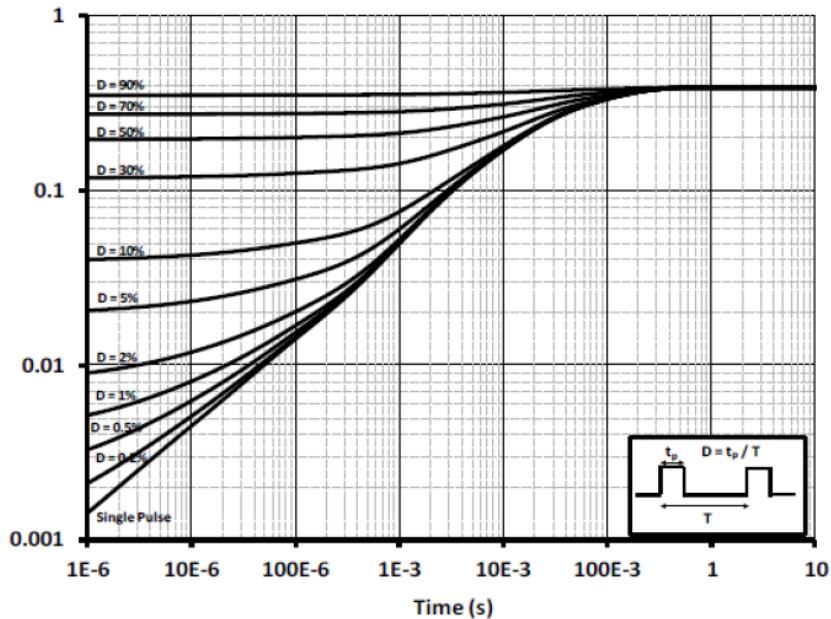


- $P_{out} \approx 14kVA$, efficiency can attain **99%** with the **DPWM1**, at $F_{sw} = 50kHz$.
- Maximum of 5% difference between measured losses and estimated losses using characterization method, for any PWM method.

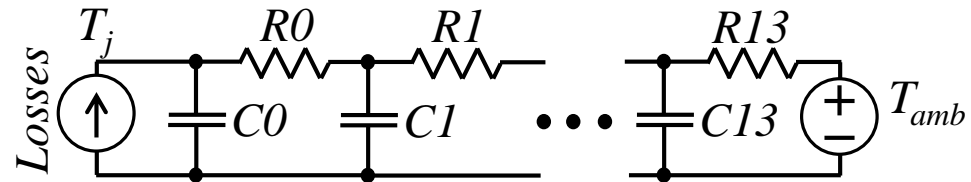
Thermal Impedance

Thermal impedance characteristics

6-pack 1200V/50A
SiC MOSFET



Thermal impedance model



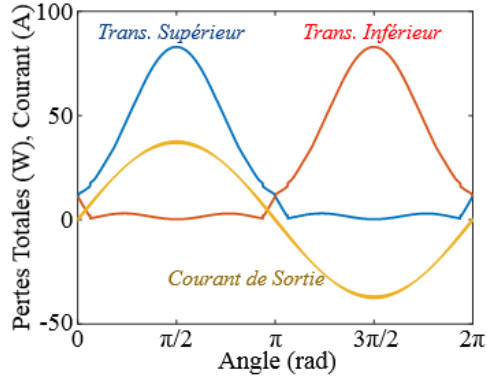
Résistance thermique (K/W)	
R0	$4,18 \times 10^{-3}$
R1	$7,49 \times 10^{-3}$
R2	$7,33 \times 10^{-2}$
R3	$1,41 \times 10^{-2}$
R4	$5,83 \times 10^{-2}$
R5	$4,24 \times 10^{-2}$
R6	$2,80 \times 10^{-2}$
R7	$2,30 \times 10^{-2}$
R8	$2,40 \times 10^{-2}$
R9	$2,42 \times 10^{-2}$
R10	$2,33 \times 10^{-2}$
R11	$2,21 \times 10^{-2}$
R12	$1,86 \times 10^{-2}$
R13	$6,80 \times 10^{-3}$

Capacité thermique (J/K)	
C0	$3,07 \times 10^{-3}$
C1	$7,93 \times 10^{-3}$
C2	$1,89 \times 10^{-2}$
C3	$9,41 \times 10^{-3}$
C4	$4,42 \times 10^{-2}$
C5	$5,33 \times 10^{-2}$
C6	$8,55 \times 10^{-2}$
C7	$1,87 \times 10^{-1}$
C8	$3,64 \times 10^{-1}$
C9	$6,51 \times 10^{-1}$
C10	1,22
C11	2,47
C12	5,01
C13	25,1

Instantaneous Losses

Instantaneous temperature difference between junction and case

SPWM



Thermal impedance of SiC Power Module

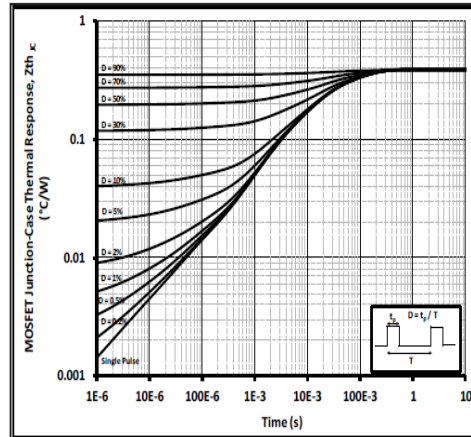
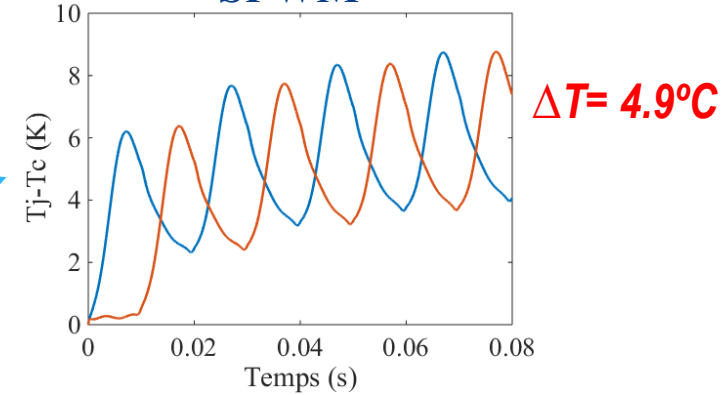
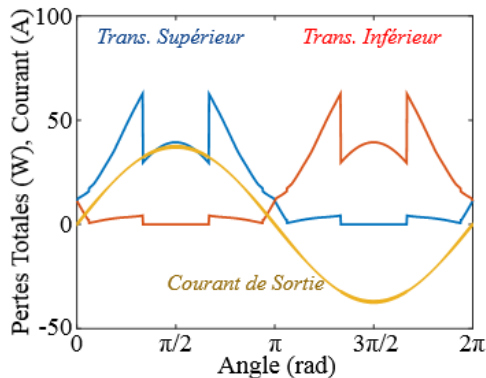


Figure 29. MOSFET Junction to Case Thermal Impedance

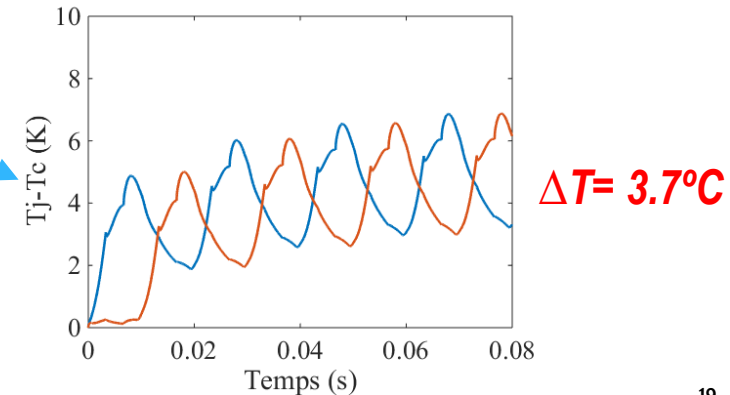
SPWM



DPWM1



DPWM1

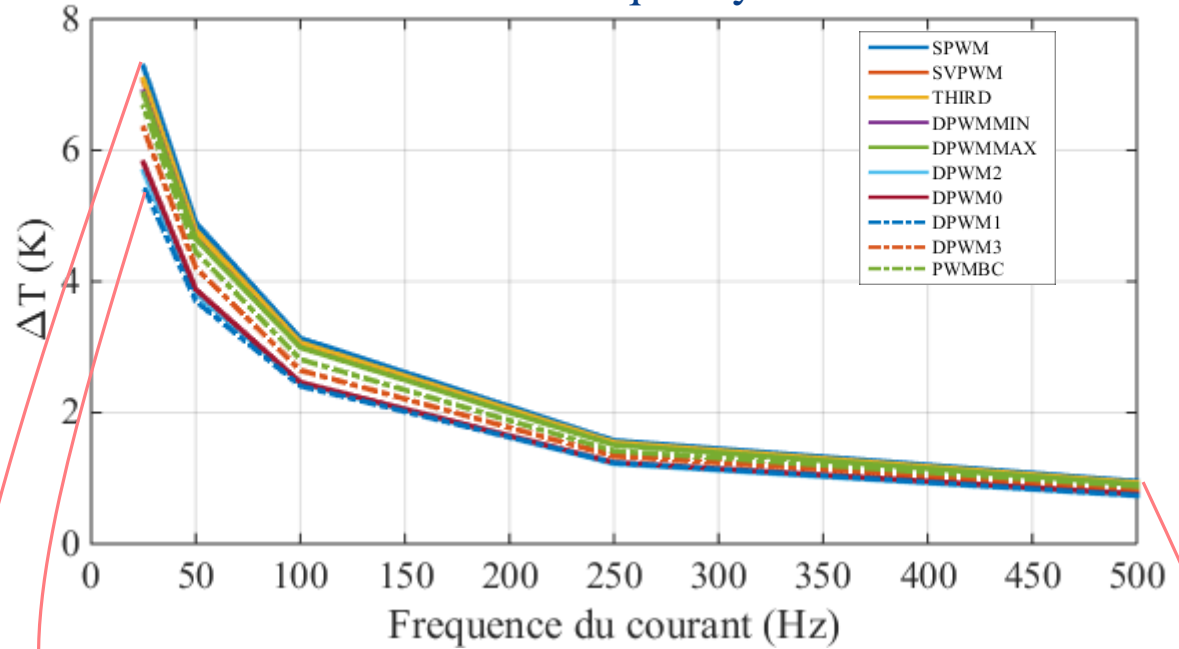


Thermal cycle amplitude of junction temperature

Operating Point

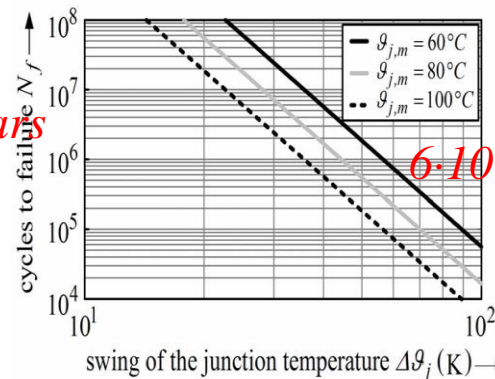
Parameters	Values
Power	15kVA
DC voltage	540V
Output current	26.3A
Mod Index	1.0
Sw Freq	50kHz
Fund Freq	50Hz
Cosφ	1
PWM method	Sinus
V_{gs}	-4V/+20V
R_g	1Ω
Deadtime	500ns
SiC MOSFET (1200V/50A)	CCS050M 12CM2

Fundamental frequency variation



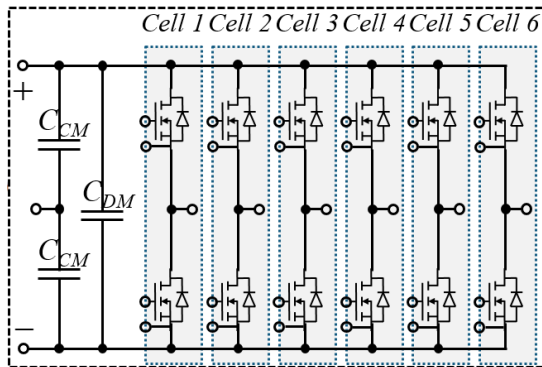
5,4K at 25Hz
 $10 \cdot 10^9$ cycles = 12.7 years

7,2K à 25Hz
 $3 \cdot 10^9$ cycles = 3.8 years

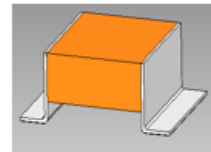


1K at 500Hz
 $6 \cdot 10^{13}$ cycles = 3800 years

Topology and Components



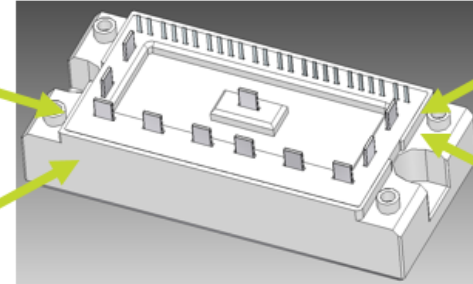
Internal Circuit of Power Module



Differential mode Capa
Ceralink 250nF



Common mode Capa
MLCC 22nF



CAO of the target module

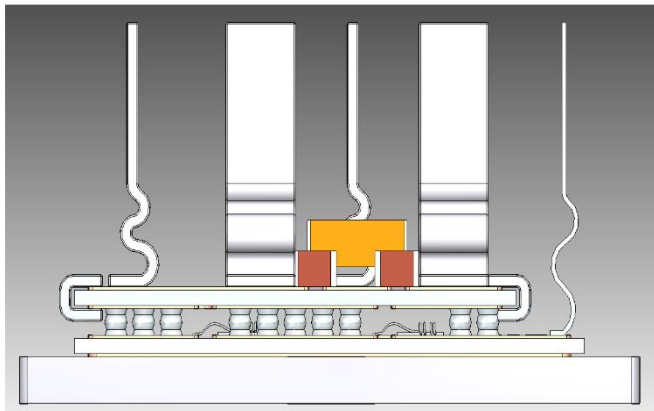


CREE MOSFET
SiC 80mΩ

Same size as
CREE 3-phase module
 $L_{stray} = 30nH$

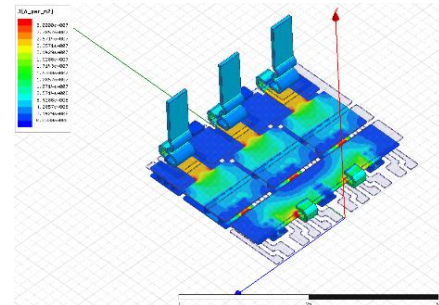
Main components

Architecture and Different Versions

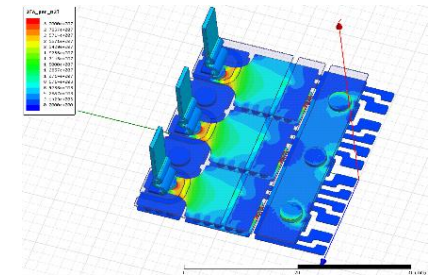


2 DBCs to decrease surface and to reduce capacitor temperatures

Design of 2 Versions



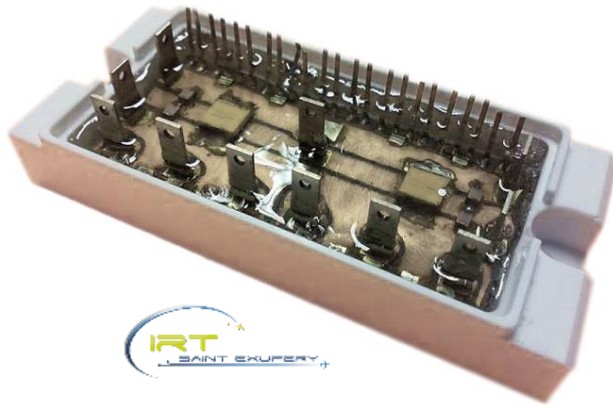
Version: Ring
 $(L_{stray} = 20nH)$



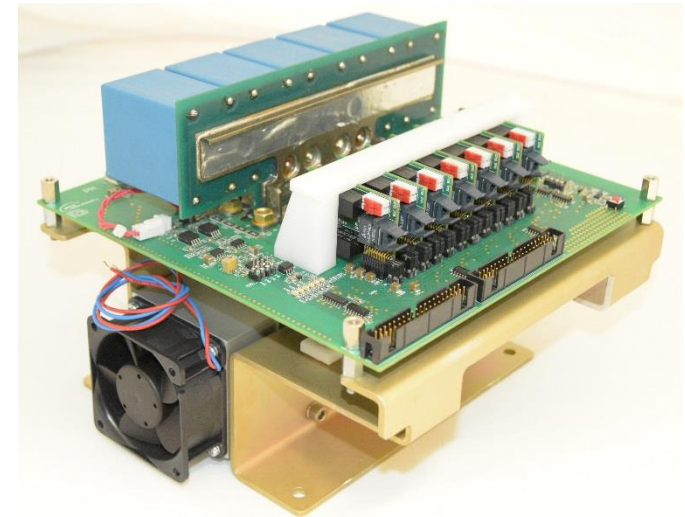
Version: Vias
 $(L_{stray} = 16nH)$

Version "Vias" made with performing DBC (Si₃N₄) to reduce parasitic inductance et resistance

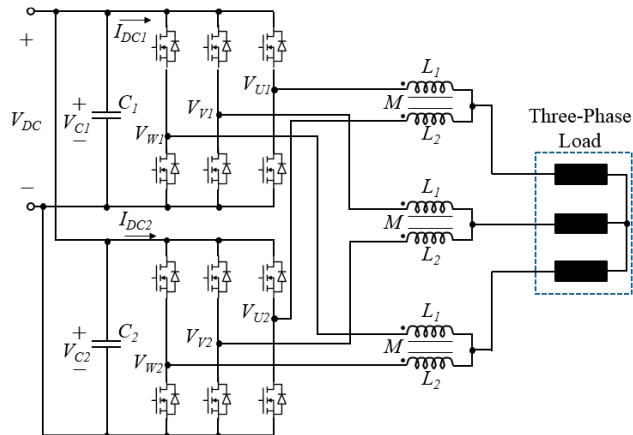
Designed SiC Power Module



Parallel Multilevel Inverter
(540V/15kVA)

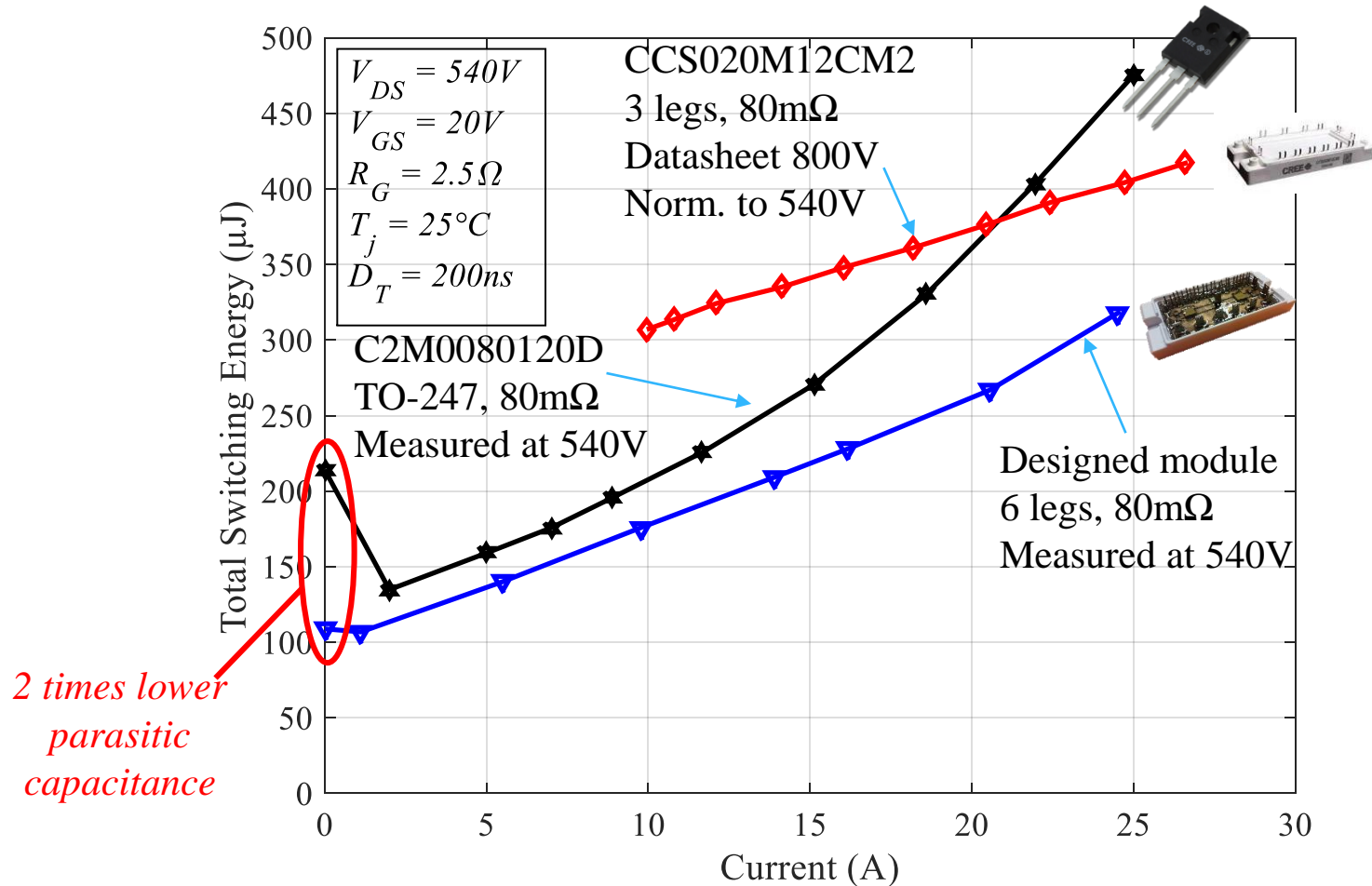


Circuit of Multilevel Converter
Using Developed SiC Power Module



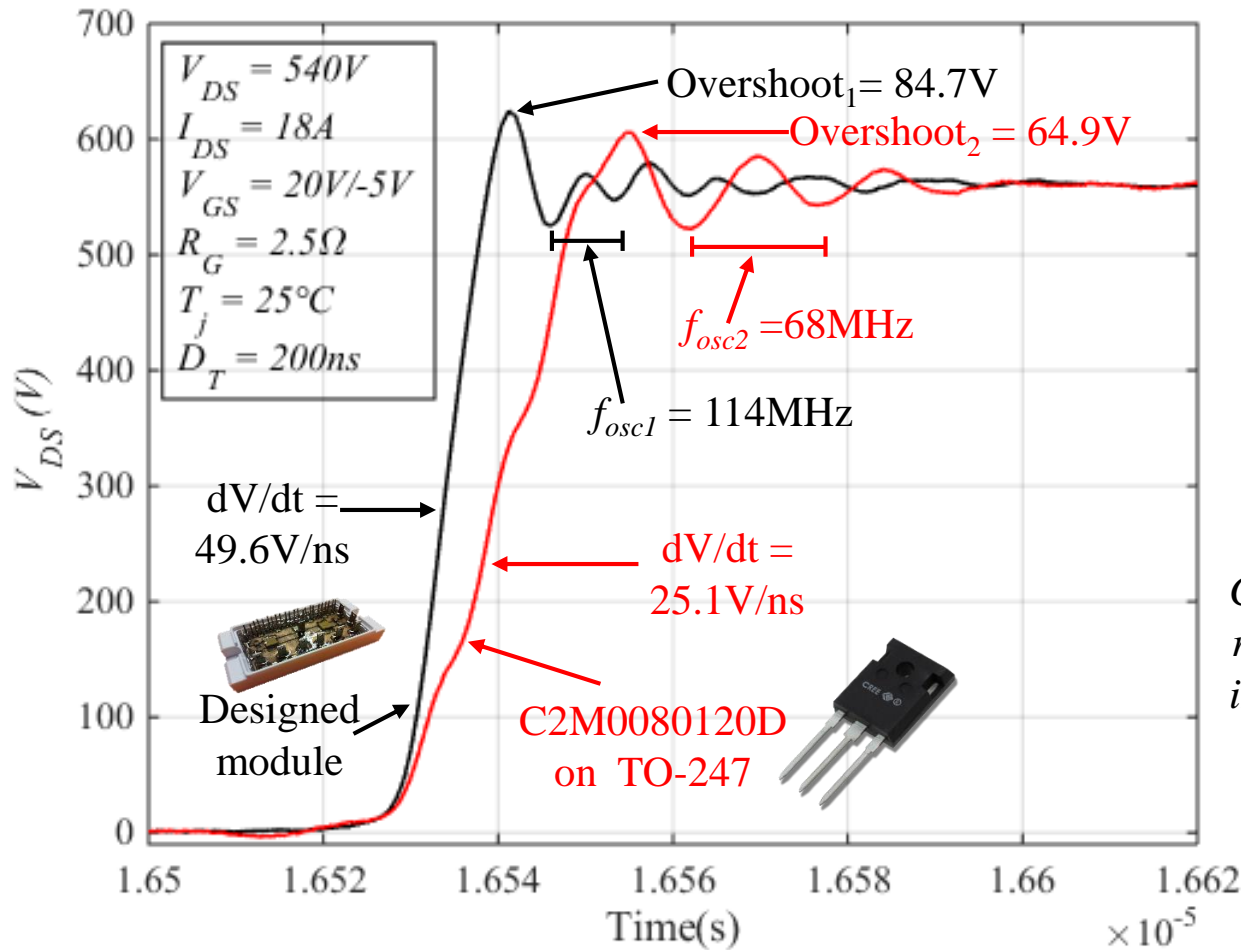
- Characterization of SiC module using the Modified Opposition Method
- Evaluation of losses, EMI and overvoltages in a double three-phase (parallel multilevel) converter using coupled inductors

Comparison between different components and modules



- Designed power module presents lower losses than commercial power module and discrete component with the same die

Comparison between different modules



$$f_{osc2}/f_{osc1} = 2.8$$

If

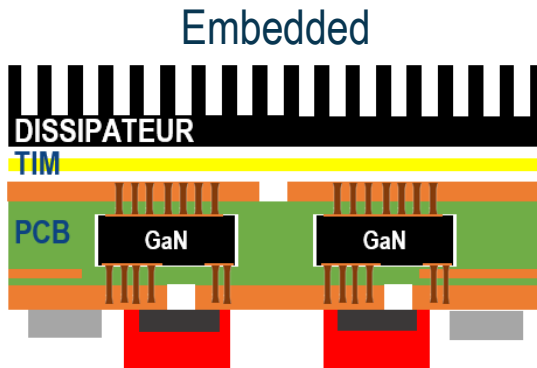
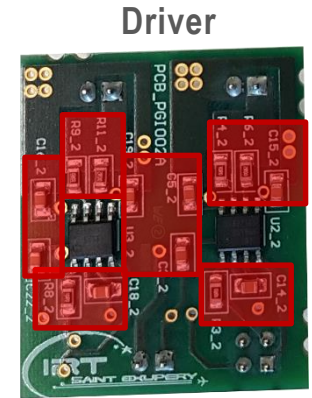
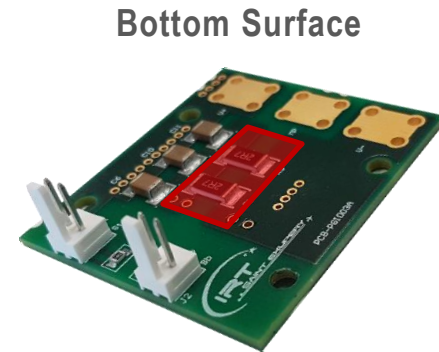
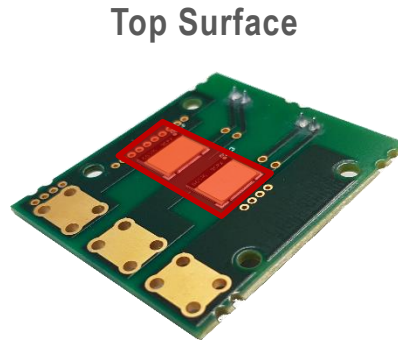
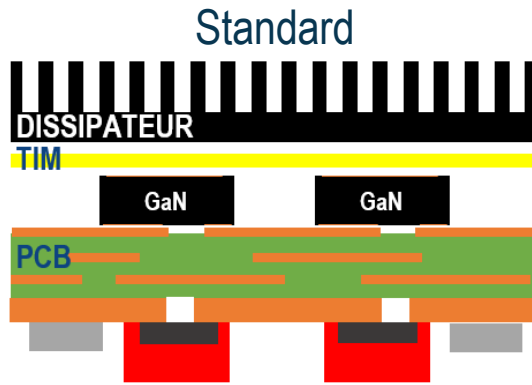
$$C_2 = 2 \cdot C_1$$

Then

$$L_{stray2}/L_{stray1} = 1.4$$

Close to theoretical ratio between stray inductances of both solutions
28nH/20nH

- Designed power module presents higher speed and low overshoot when compared to discrete component using the same die



Goals:

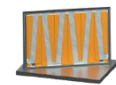
- Increase power density
- Improve thermal and electrical performance

Packaged Component



GS66516T
60A, 25mΩ
Top cooling

Bare Die

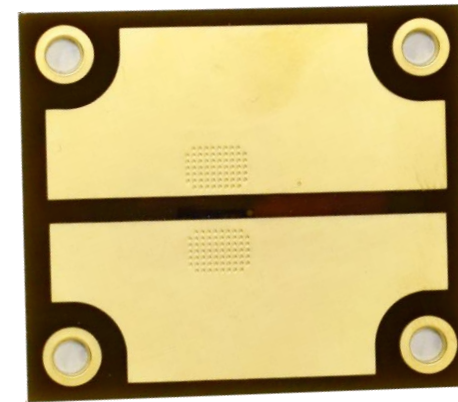
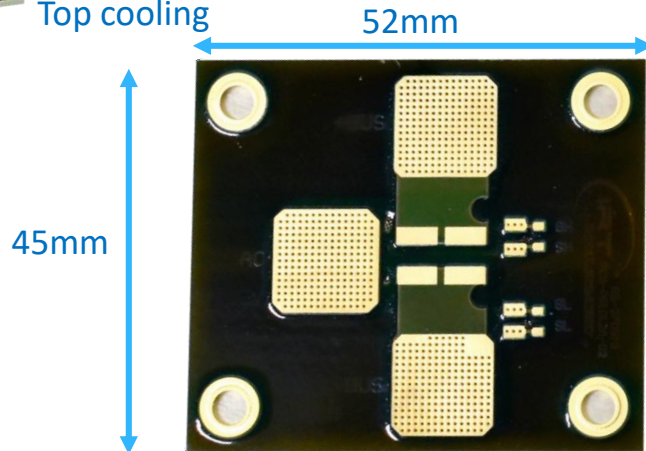


GS-065-060-2-D
60A, 25mΩ



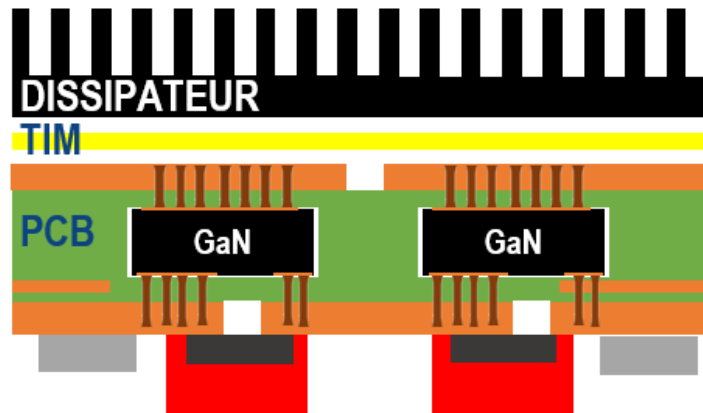
GS66516T
60A, 25mΩ
Top cooling

Embedded GaN pre-packaged die



Thermal pad
surface
731mm²

Copper
thickness
250μm

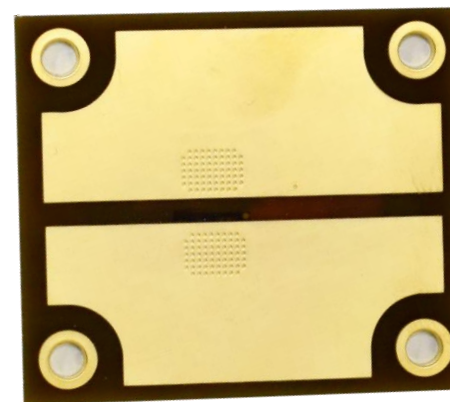
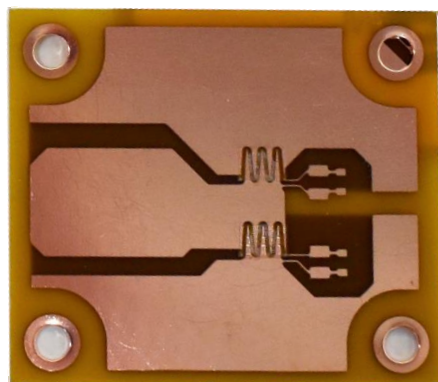


- Good thermal resistance
- Very low inductance



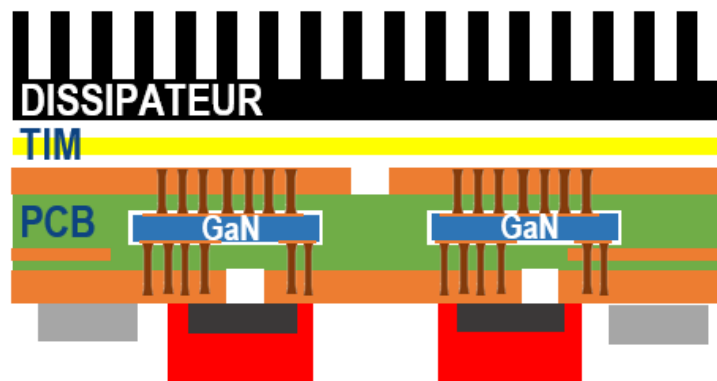
GS-065-060-2-D
60A, 25mΩ

Embedded GaN bare die



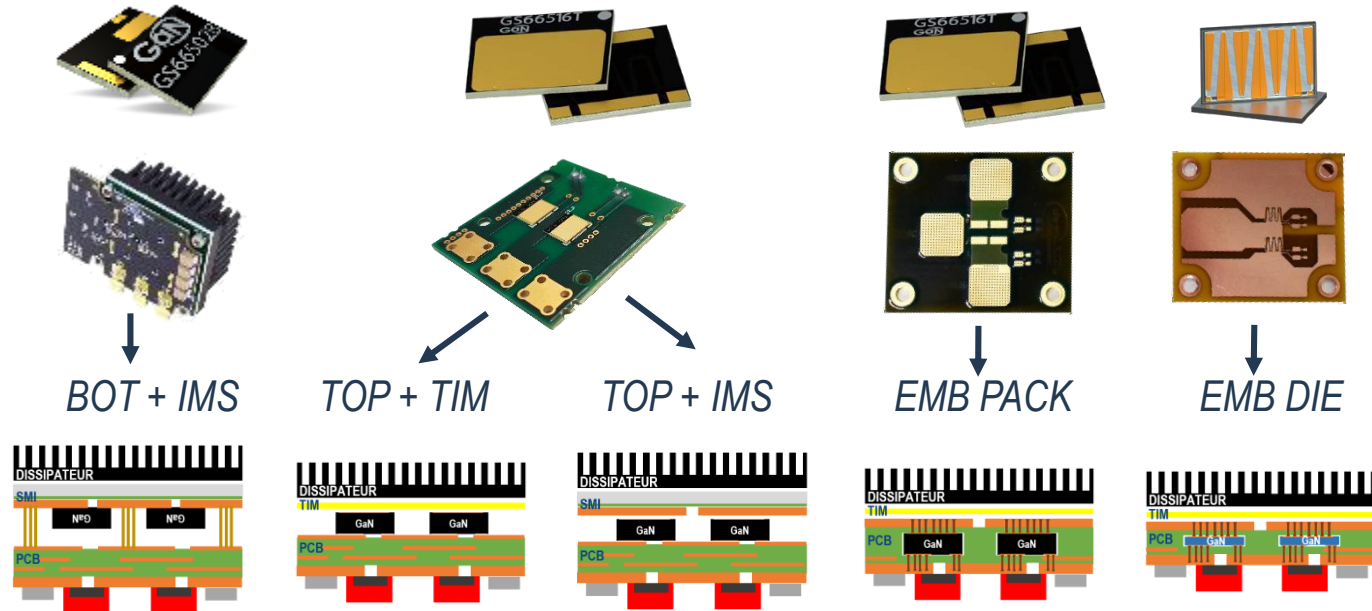
Thermal pad
surface
XXmm²

Copper
thickness
250μm



- Very good thermal resistance
- Very low inductance

Comparison



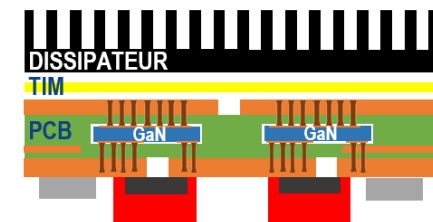
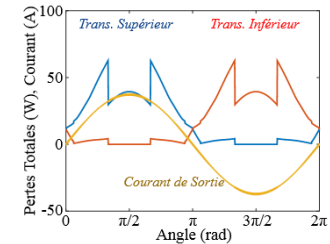
	BOT+IMS	TOP+TIM	TOP+IMS	EMB PACK	EMB DIE
Thermal resistance	Worst	Good	Very Good	Very Good	Best
Electrical performance	Worst	Good	Good	Best	Best
Power Density	Good	Regular	Regular	Best	Best

Expected

- Reliability of such packaging is one of the following subjects at IRT

Conclusions – EPowerDrive Project

- **EPowerDrive** project at IRT Saint Exupery proposes technologies, models and tools to **increase power density and efficiency** of the whole Power Drive System using WBG semiconductors (Silicium Carbide SiC and Gallium Nitride GaN).
- **Reliability** of Power Drive Systems using SiC and GaN can be improved by reducing **overvoltages, switching speed, losses** and **thermal cycles** amplitude. Some works at EPowerDrive aim on reducing these values.
- **PWM methods** improve some characteristics in three-phase converters such as losses and thermal cycle amplitudes.
- **Integrating capacitors inside SiC** power module reduce overvoltage and losses.
- **GaN embedded inside PCB** reduce thermal resistance as well as overvoltage. Reliability of such “packaging” is being studied by IRT.





Thank you for your attention

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