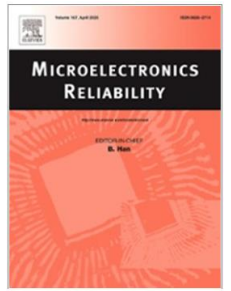
NRTW 2025

National Reliability Technology Workshop

Mercredi 19 et Jeudi 20 mars 2025 | GANIL – Bd Henri Becquerel, 14000 Caen

Investigation sur la durée de vie à basse température des grilles pour un p-GaN HEMT



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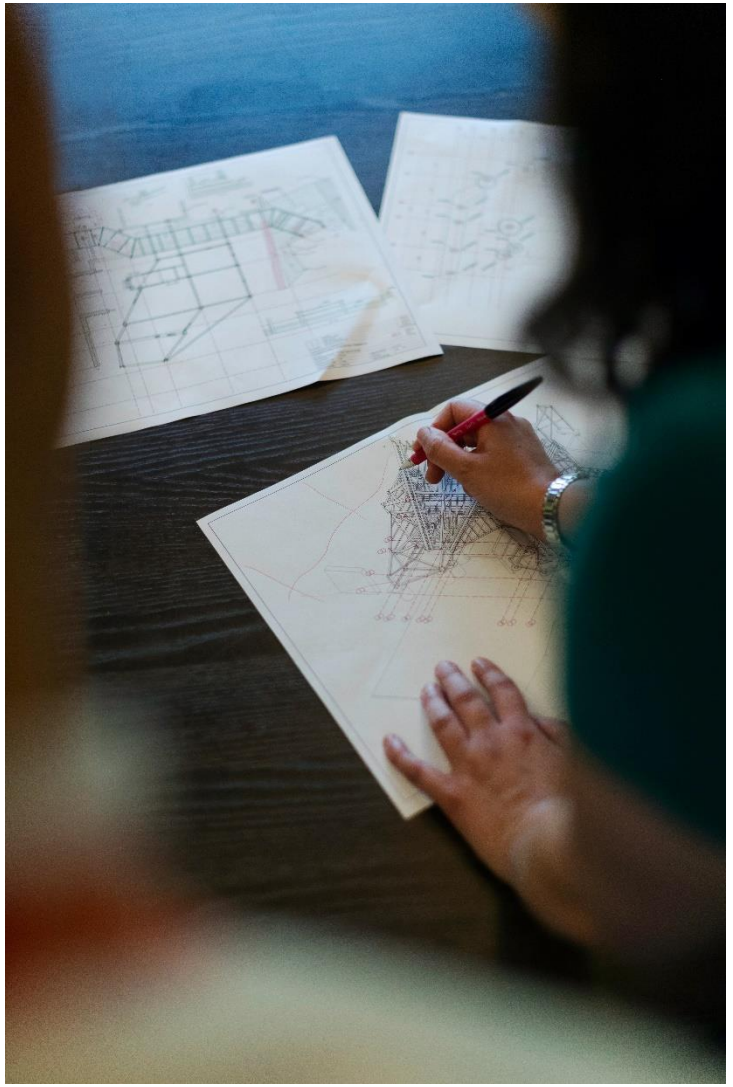
Organisé par :

Agenda

- Alter Technology France presentation
- GanRET One pager
- Design Of Experiment
- Gate Lifetime Test:
  - Temperature Dependance
  - Voltage Dependance
- Physical explanations
- Conclusion



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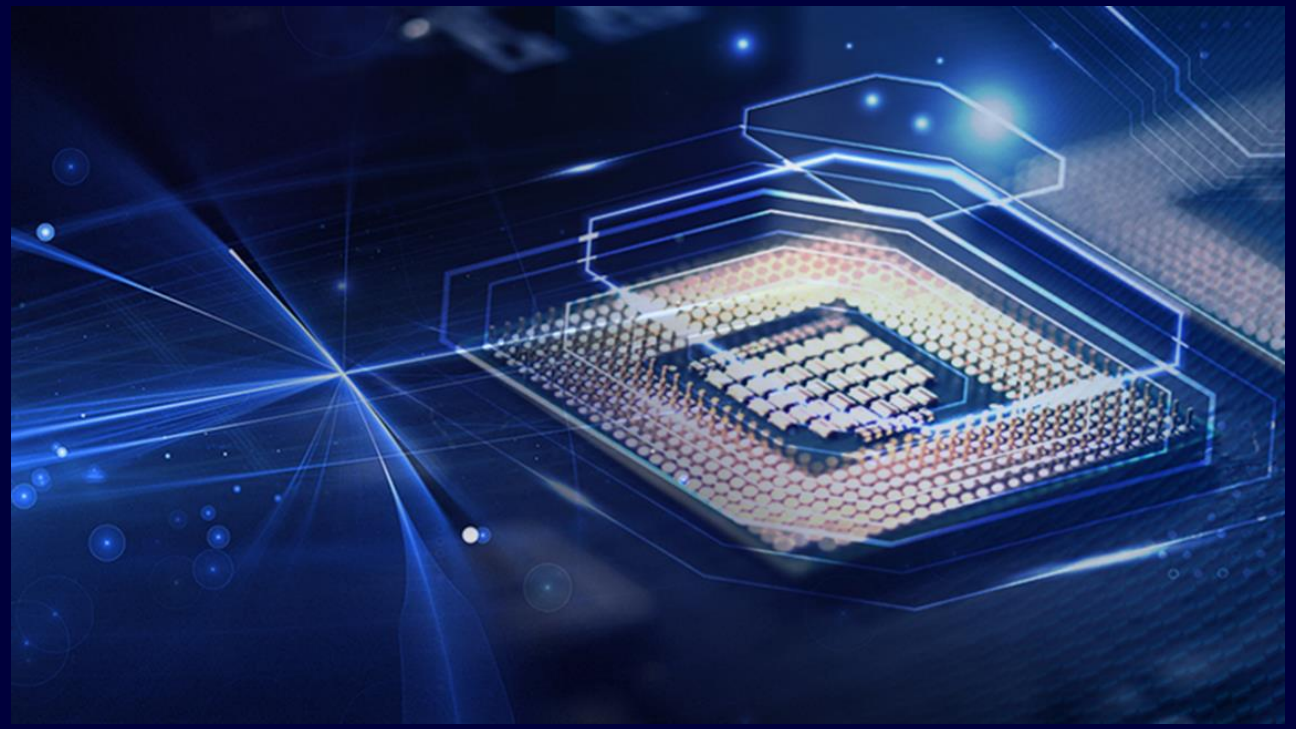
ALTER FRANCE

Inspired by Knowledge



TÜV NORD Group

Figures, data, facts

The TÜV NORD GROUP at a glance

1,451.8

Million Euro sales

12.238

Employees worldwide

TÜVNORDGROUP

TÜVNORD · DMT · ALTER · TÜVIT

4

Core Brands
in the Industrial Services, Mobility, Training, Engineering and Natural Resources, Aerospace and IT business units

100

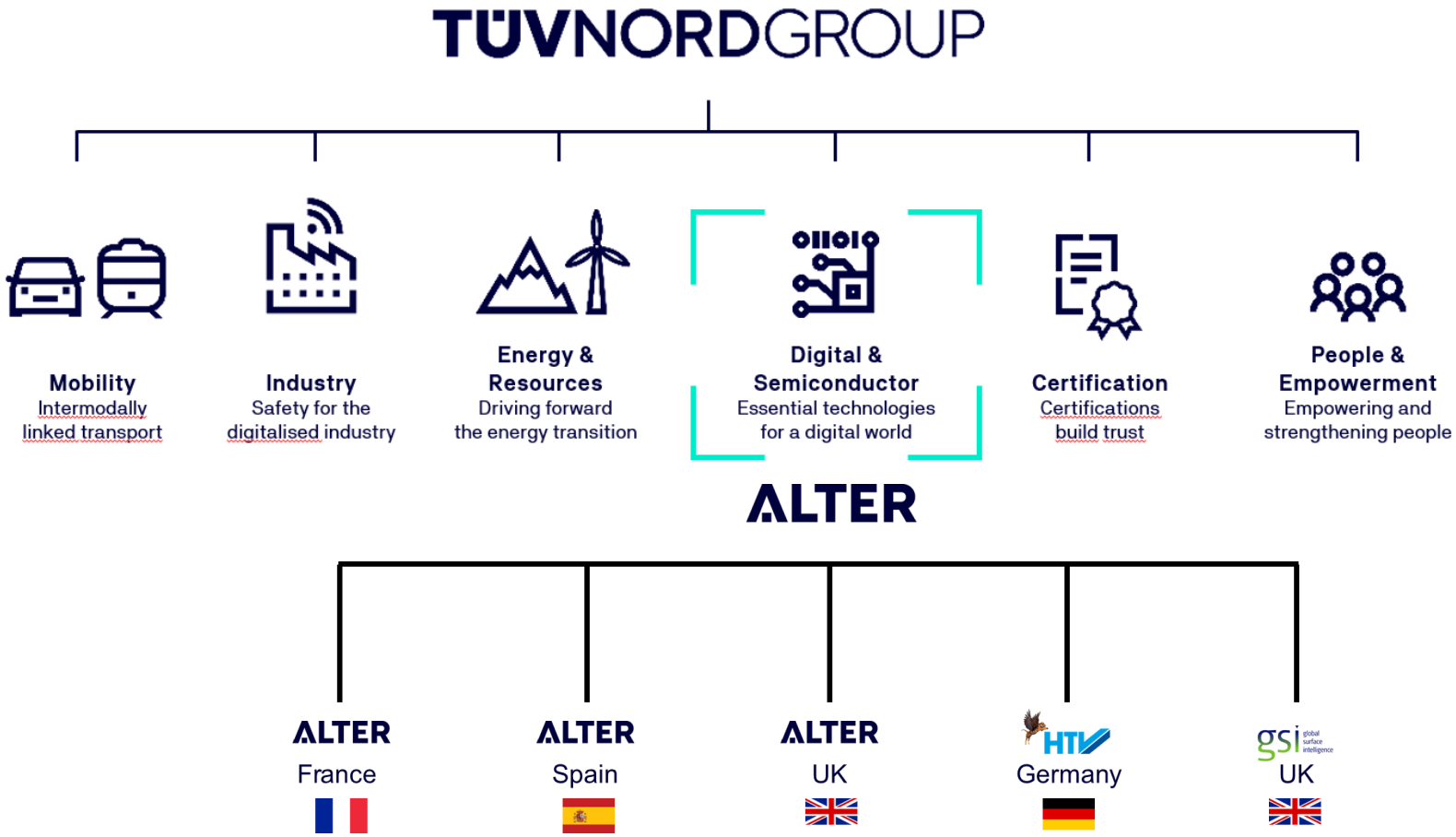
Active in 100 countries

82

Group Companies

ALTER Group

Figures, data, facts



ALTER France

ALTER France at a glance

14

Millions euros Revenues

10%

of Revenues Invest

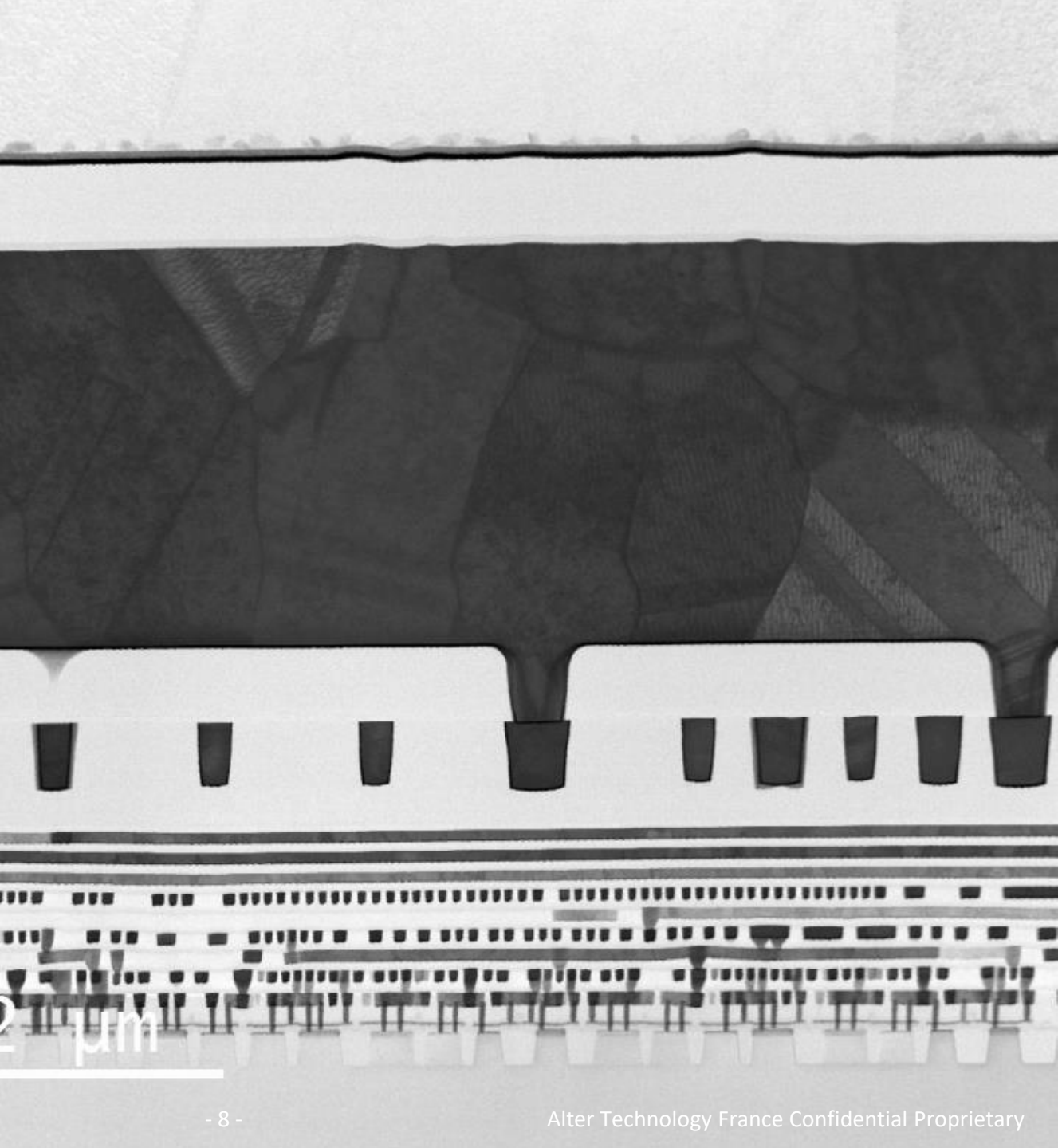
59

Employees

1600

M2 Laboratories

Business sectors



Technology Analysis

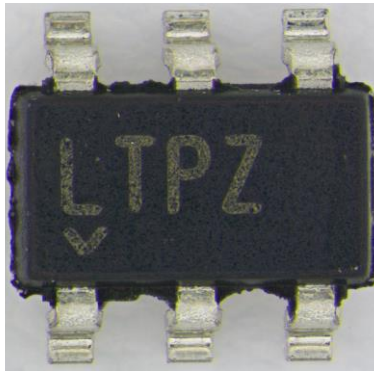
Our Technology Analysis Lab is in charge of performing deep-dive Analysis on product construction or product failure.

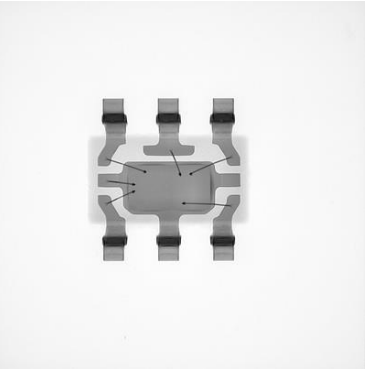
The laboratory mission is to identify potential weakness or root cause of malfunction on part or system.

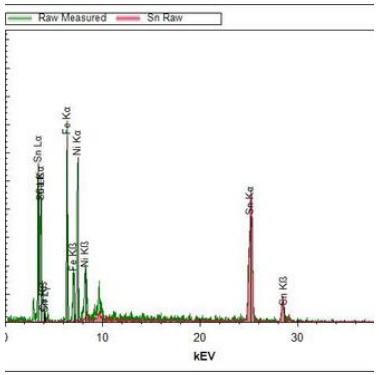
Counterfeit

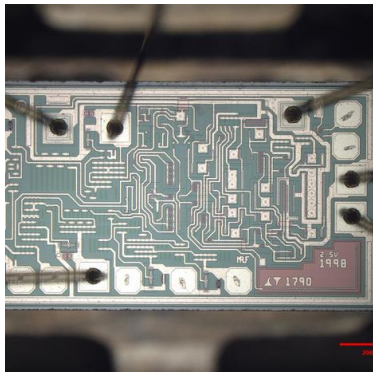
Alter Technology France provides a full suite of counterfeit semiconductor detection methods to assist our customer in making a determination regarding IC authenticity.

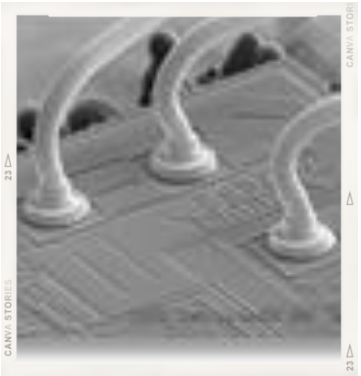
Authenticity detection can be performed according to company's specifications or based to industry standards such as SAE A6081, SAE AS5553 and IDEA-STD-1010B.

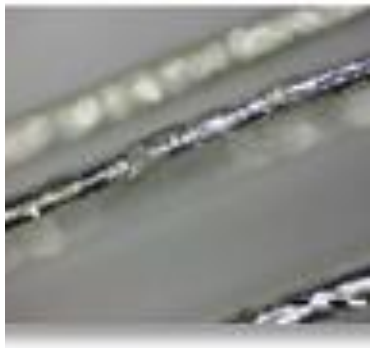










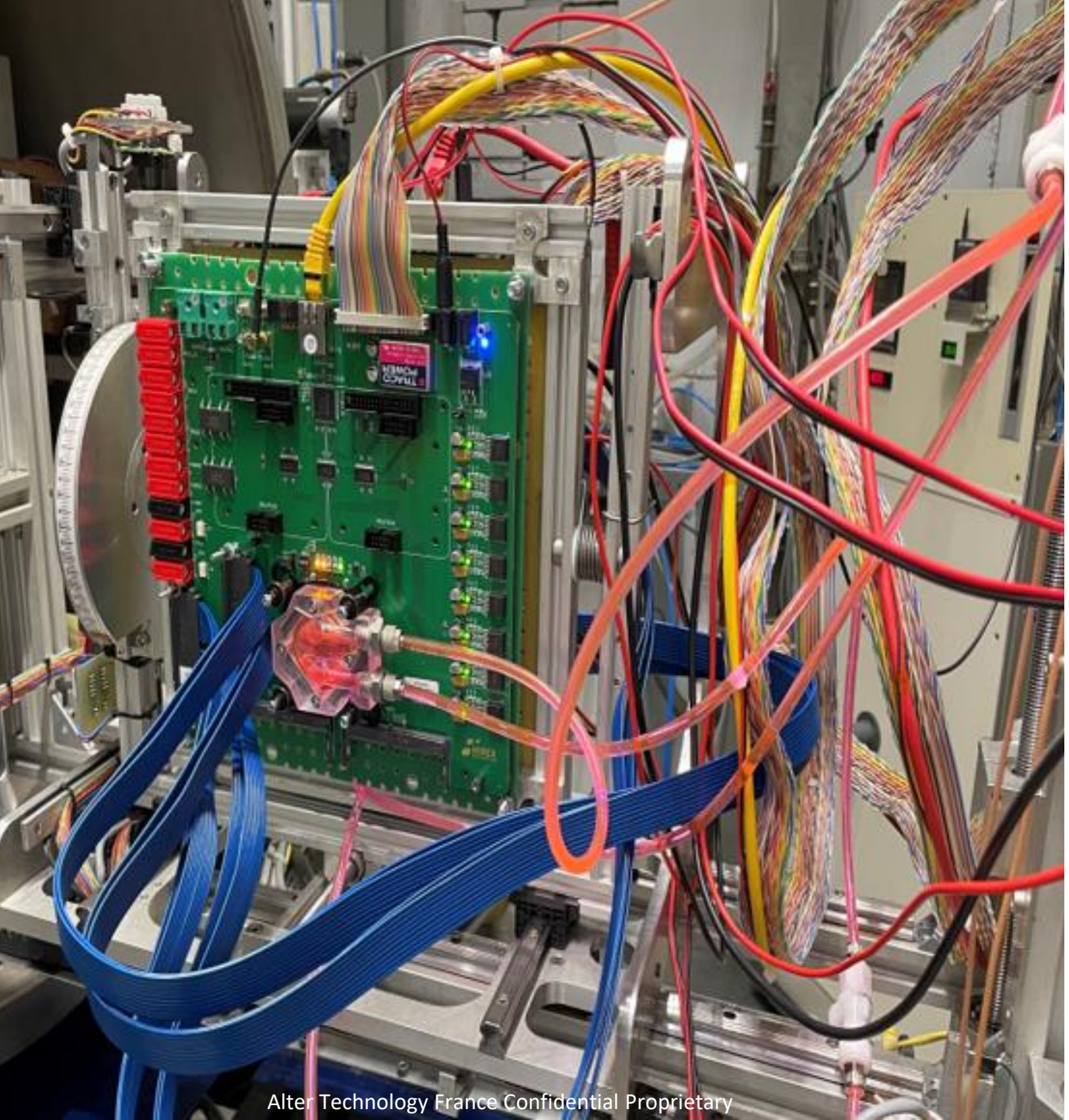


Total semiconductor testing

Acting as an NPI (New product introduction) facility offering semiconductor Electrical testing, components qualification & characterization.

Alter Technology France's electrical test services encompass both final test and probe. Certifying the semi-conductor product against their applications.

One Stop-shop

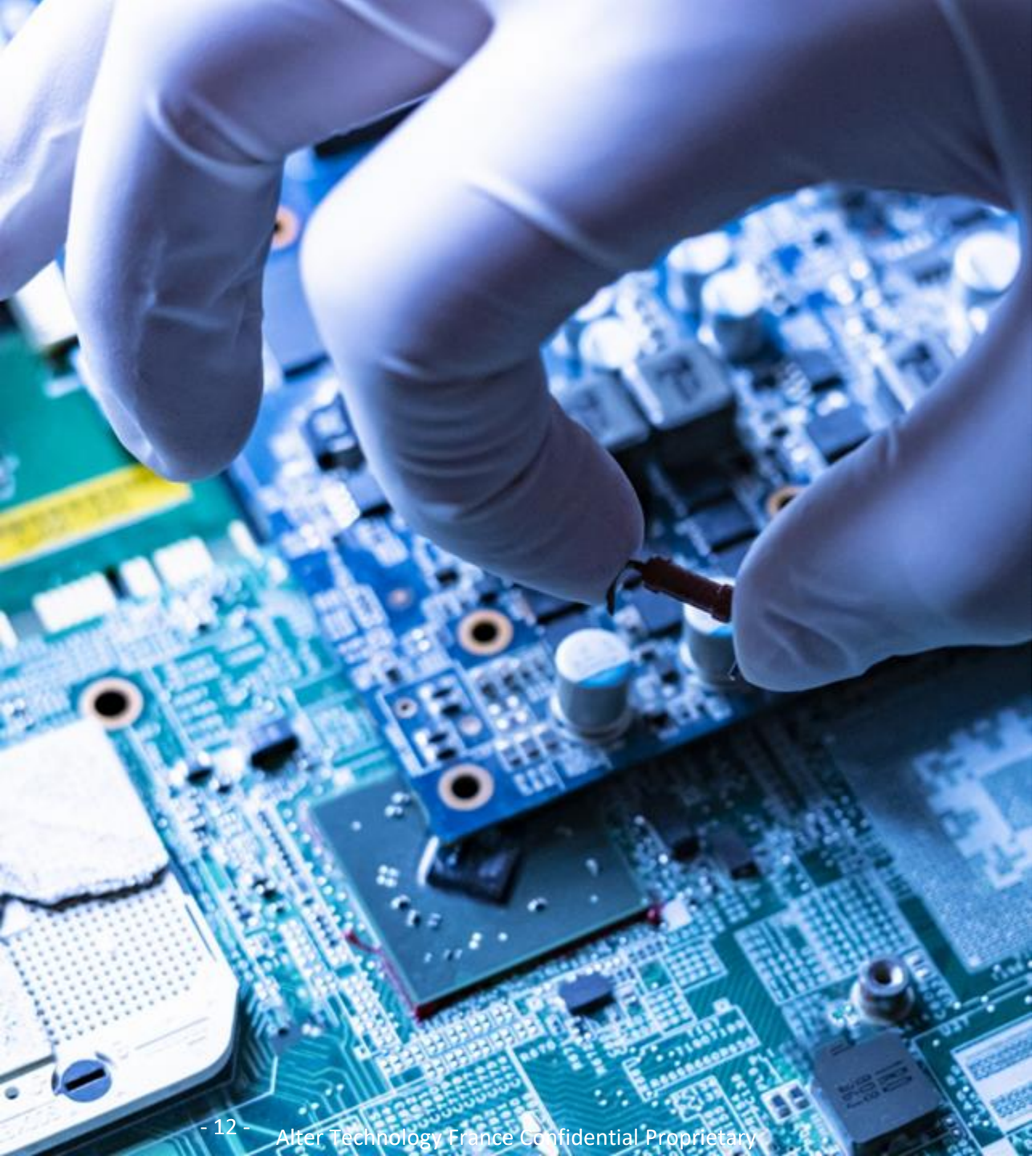


Radiations services

Engineering radiations involve using standard software tools and in-house software to quickly assess how semiconductor devices behave.

In addition to these activities, Alter Technology France conducts radiation testing on various semiconductor components, packages, modules and boards.

This testing assesses single event effects, total dose, and displacement damage by exposing them to heavy ions, protons, neutrons, and cobalt 60 irradiation or using laser and XRAY equipment.



Procurement

Parts procurement through IDM (Integrated Die Manufacturer), distributor partners or in partnership with Alter Technology France group with traceability and testing services added involves the process of sourcing and acquiring semiconductor components for electronic devices while ensuring their authenticity, quality, and performance through traceability and testing.

This comprehensive approach helps mitigate the risks associated with counterfeit or substandard components and ensures that the acquired semiconductors meet the required specifications and standards.

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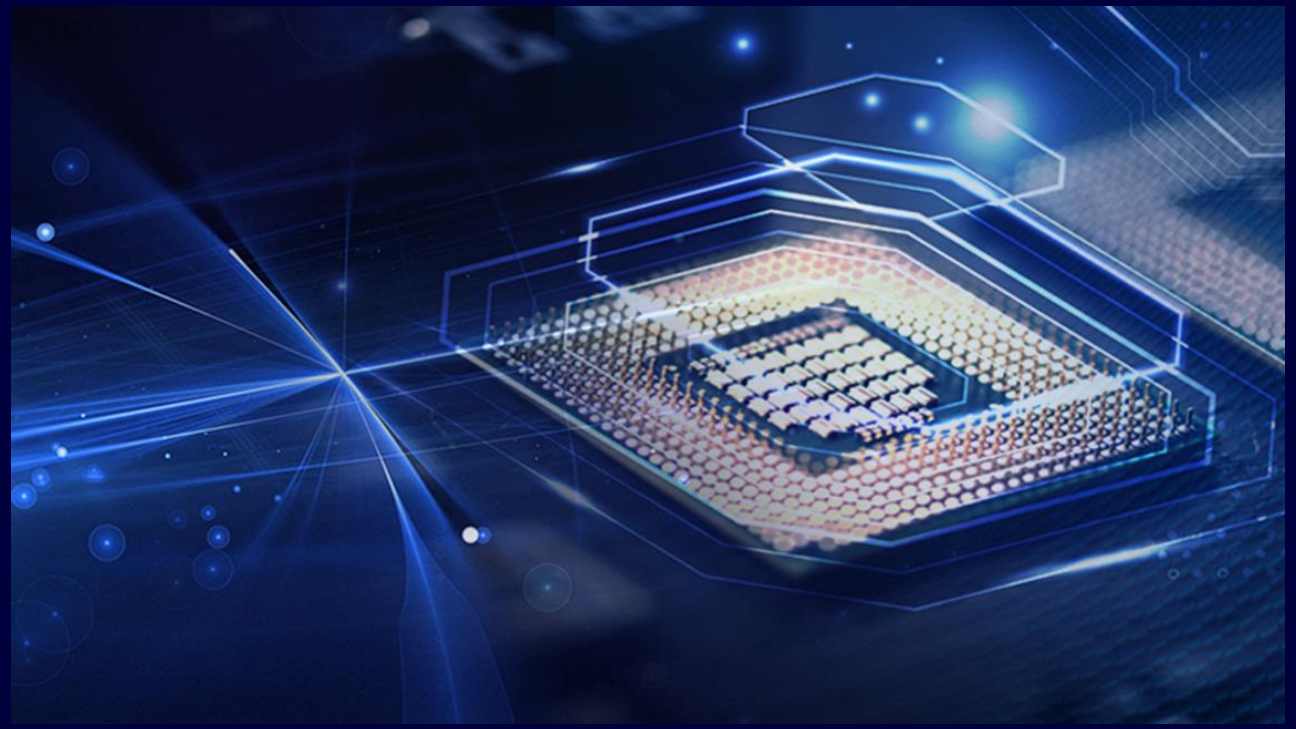
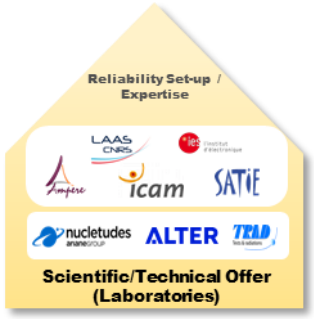


GaNRET One Pager



STMicroelectronics Wise integration

cnes DGA

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GANRET

GaN Reliability Evaluation for Transport

Enabling GaN based power electronic insertion into severe environmental constrains chain

An end-user driven project…

6 M€ | **48 months** | **15 partners** | **4 PhDs + 2 postdoc**

Excepted Outcomes

- **Understanding of underlying PoF**: Identification of the **critical stressors and indicators** specific to the given usage mission profile
- **Test-for-GaN**: Definition of **test methodologies** adapted to GaN technology and support the definition of dedicated **qualification protocols**
- **Design-for-GaN:** Margin aware design rules and methodology for risk assessment and mitigation (design recommendation, safety margins, etc.)
- **Manufacturing-for-GaN:** Support GaN ODM to **improve manufacturing** technology maturity ⇨ Technology improvement

Work Packages

WP1: DUT & Mission Profile Specification
- Market analysis
- DUTs selection
- Mission profile analysis

WP2: Exploration phase
- Measurement/stress protocol
- Electrical characterization
- Thermal investigation

WP3: Reliability Investigation
- Static aging tests
- Dynamic aging test
- Short-circuit

WP4: Radiation Immunity Assessment
- Alternative test methodologies
- NDT methodology development
- Mutual effect reliability-radiation

WP5: Exploitation and Capitalization
- Reliability tool for risk assessment
- Lighthouse initiatives
- Supporting standardization *entities*

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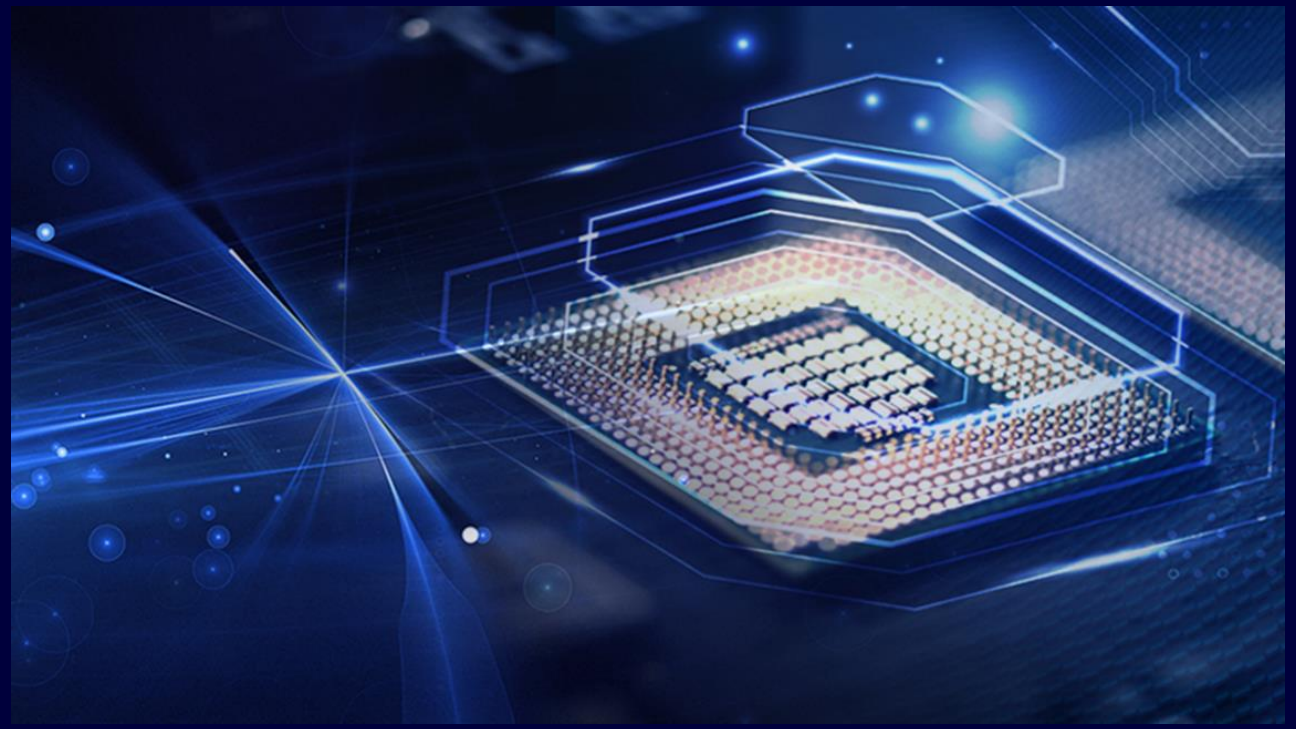
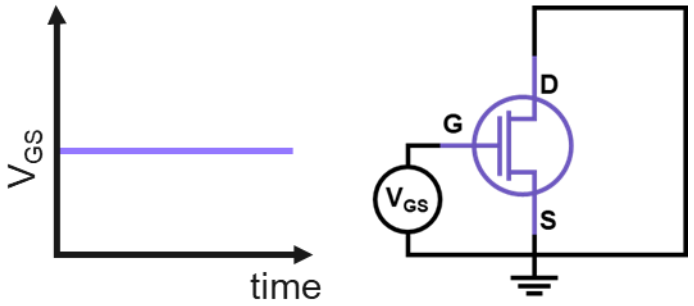
Gate lifetime investigation at low temperature for p-GaN HEMT



Maroun ALAM

maroun.alam@irt-saintexupery.com

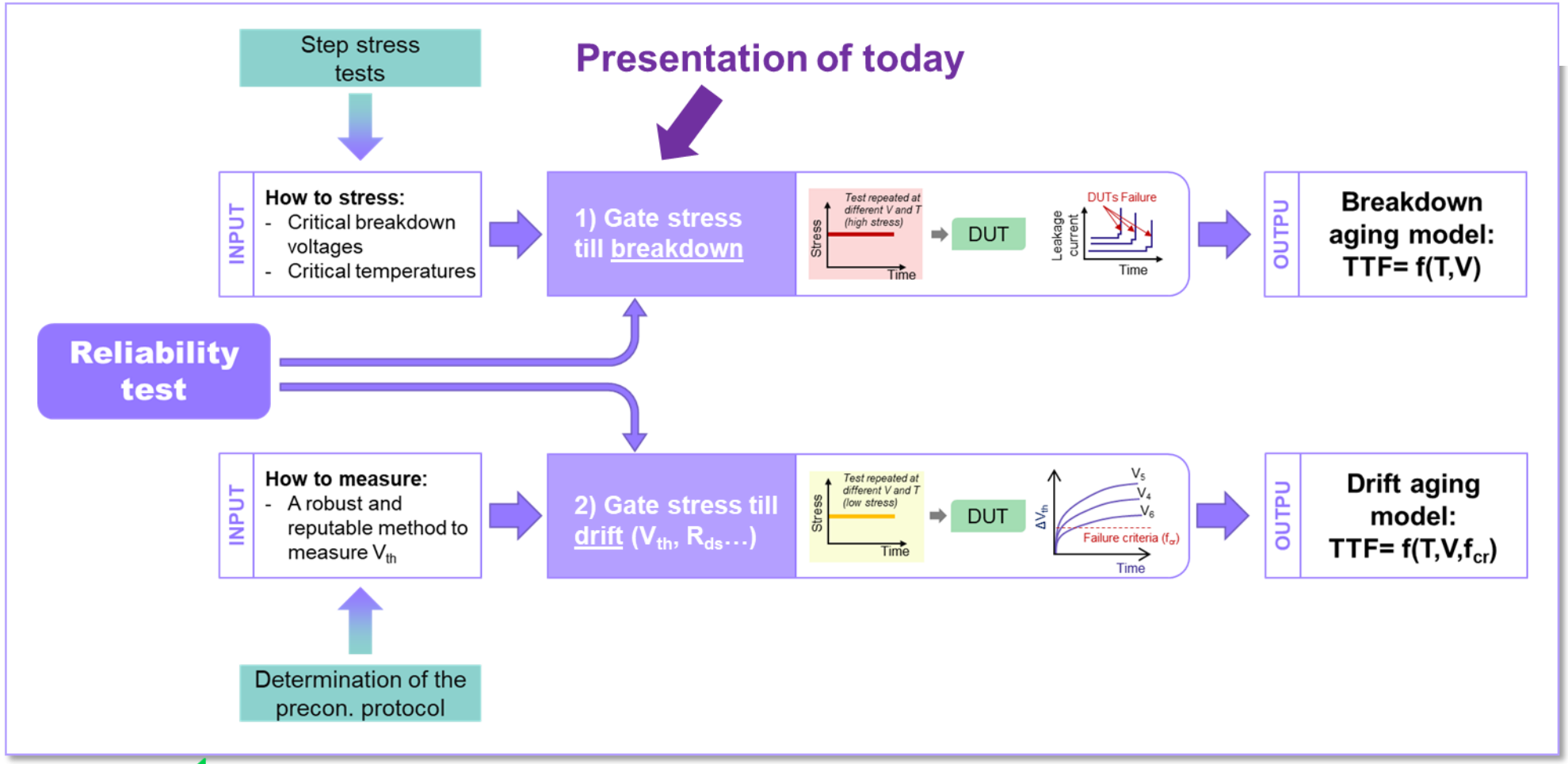
Gate Lifetime: The Existing Qualification Protocol

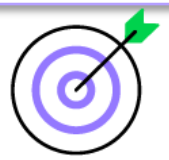


- To qualify the gate, Si standard used test protocol is the so-called High Temperature Gate Bias (HTGB – 1000h @ 150°C)
- If during the test the **gate breakdown** nor **V_{th} drifts** are observed → the component is qualified
- The test is performed at **high temperature**, because for Si-based technologies this usually represent the **worst case**

But what about p-GaN devices? What is the worst case? High or low temperature?

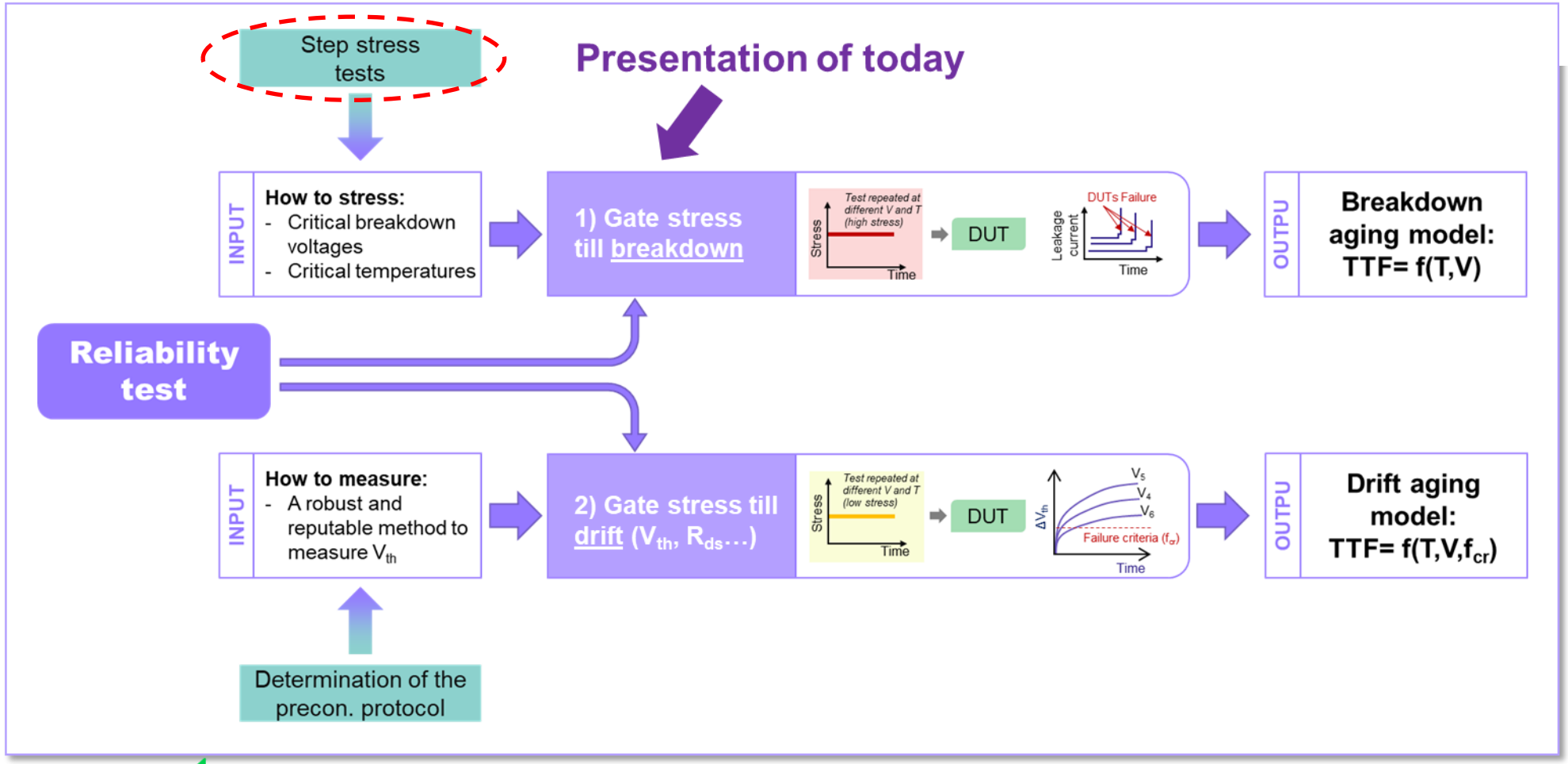
Context and Objectives

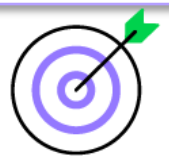




- ✓ Evaluate gate lifetime and understand influence of temperature
- ✓ Retrieve aging models for lifetime predictions

Step-Stress presentation





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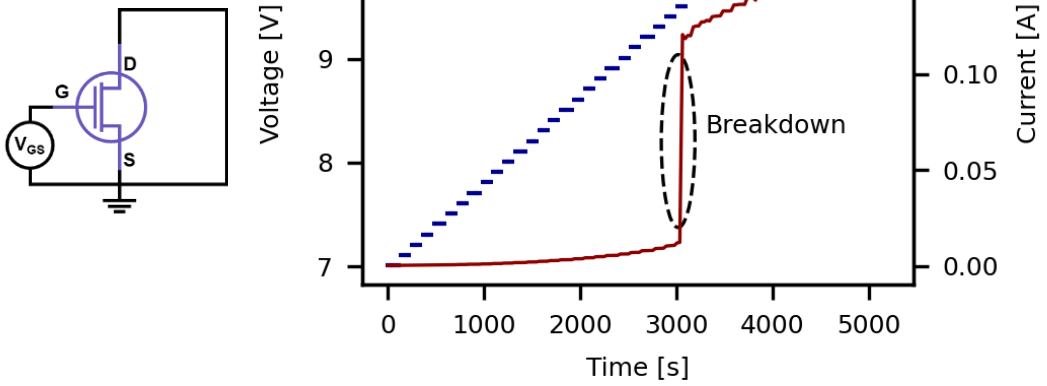
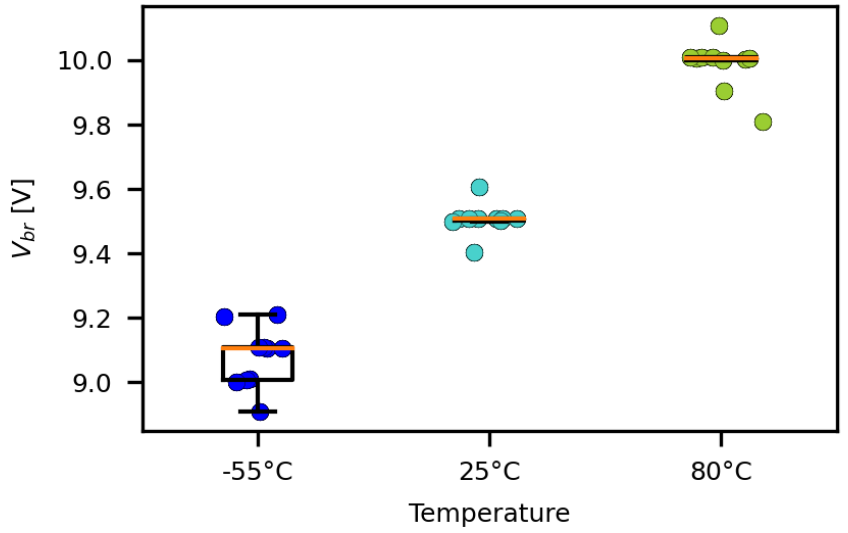
Preliminary investigation:



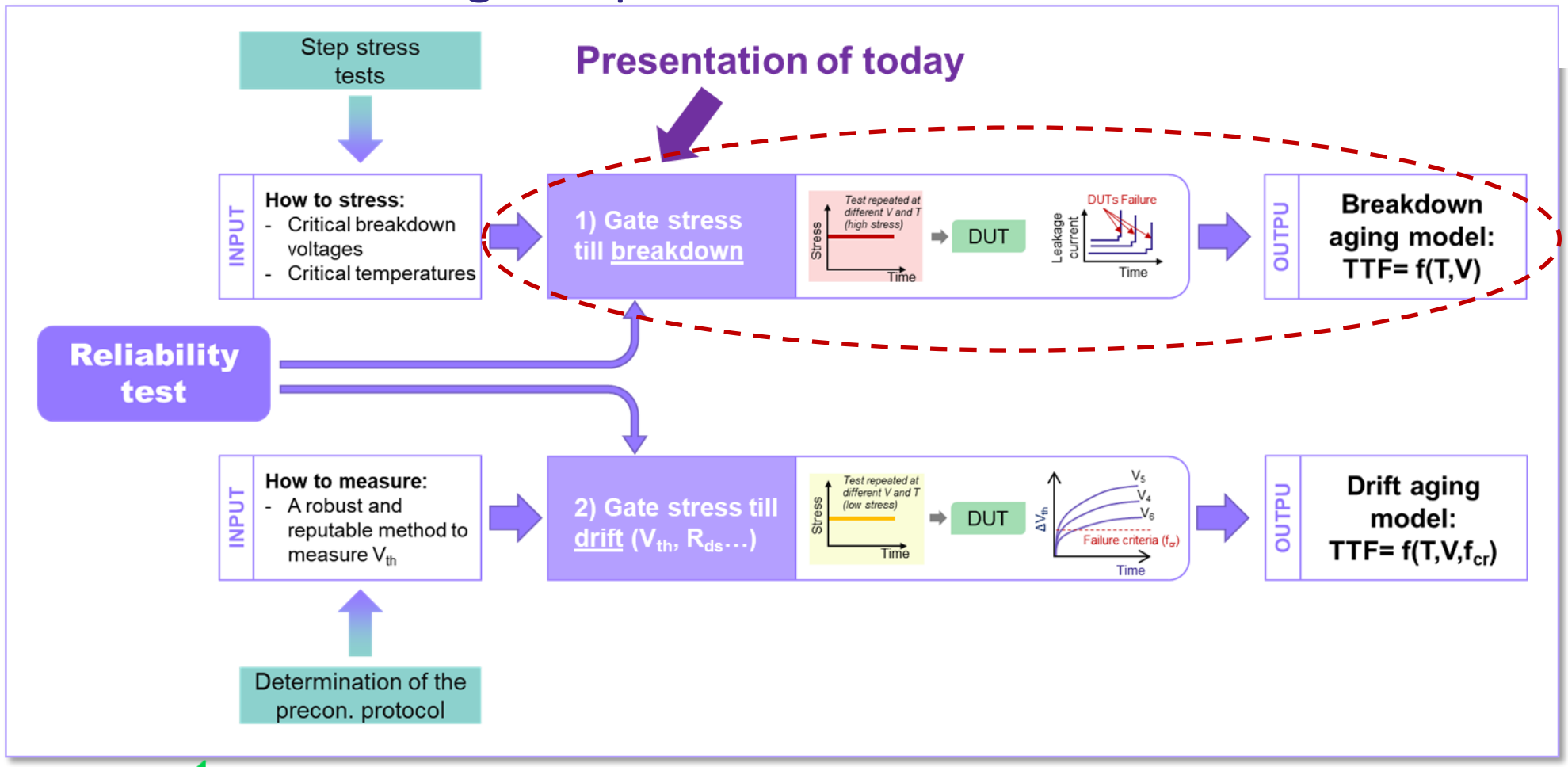


- Step-stress test was conducted to determine the gate breakdown voltage at different temperatures.
- This determined the test plan for evaluating static gate lifetime by identifying breakdown points at each temperature.
- V_{GS} was incremented in 0.2 V steps, starting from 7 V, with each step lasting 2 minutes, until gate breakdown was observed.
- The breakdown was indicated by a sudden increase in the leakage current.

Gate breakdown voltage increases with higher test temperatures, indicating that gate lifetime diminishes at colder temperatures.

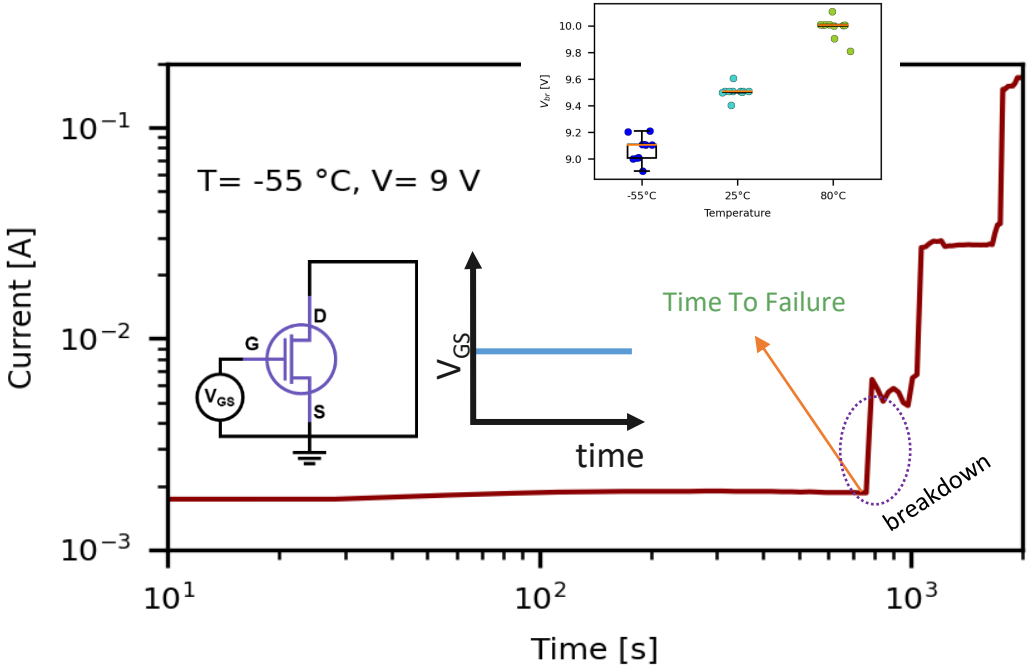
Gate Lifetime Tests

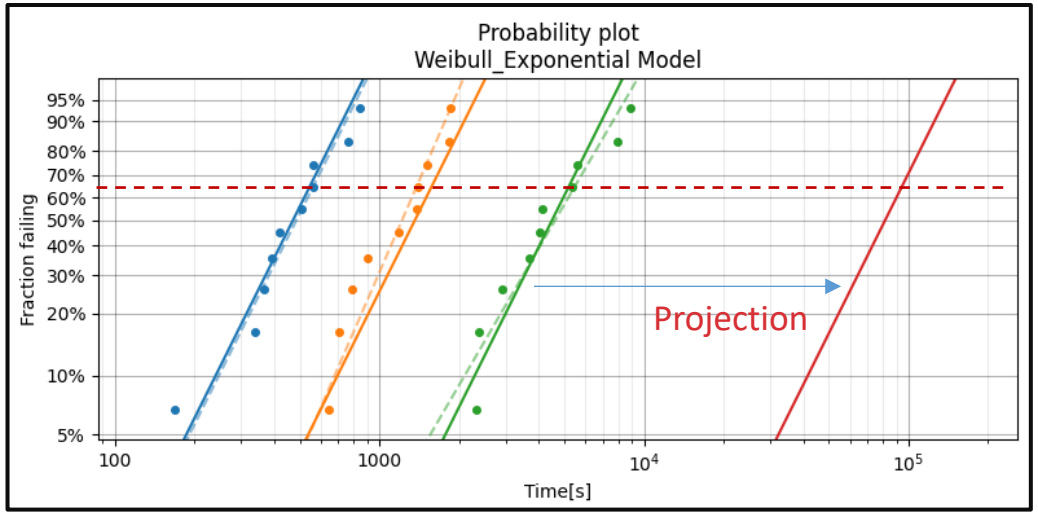
Static stress on the gate up to failure



- ✓ Evaluate gate lifetime and understand influence of temperature
- ✓ Retrieve aging models for lifetime predictions

Gate lifetime: Test protocol



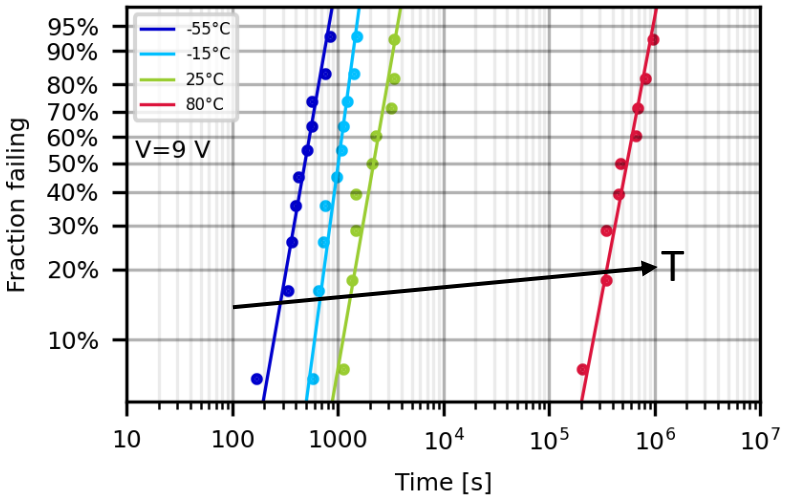


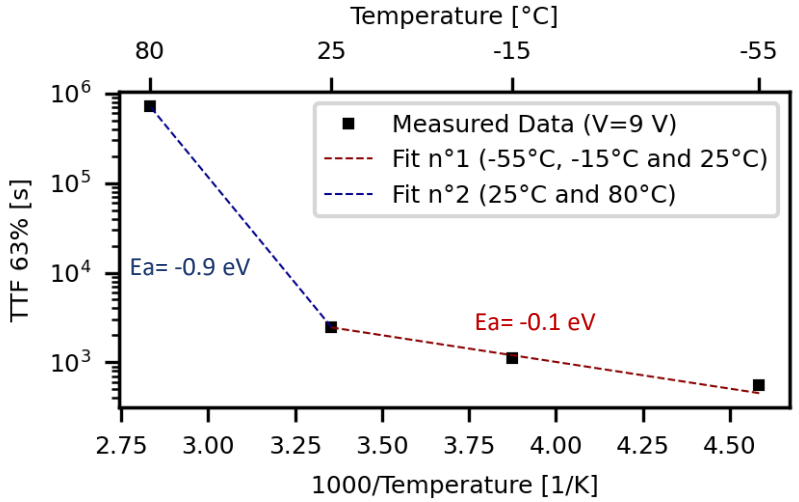
- For a single component → Time To Failure: time at which the current suddenly increase for the first time
- For projections estimation → Mean Time To Failure: time at which the 63.2% of the DUTs has failed

To study the influence of voltage and temperature on gate lifetime, measurements were conducted at 8 V, 8.5 V, and 9 V across the following temperatures: -55 °C, -15 °C, 25 °C, and 80 °C.

Temperature-dependent Gate lifetime

- To evaluate the effect of temperature on gate lifetime, measurements were taken at the following temperatures: -55 °C, -15 °C, 25 °C, and 80 °C for V_{GS}= 9 V.
- The results were plotted using a Weibull distribution, showing the shortest time to failure at -55°C.
- The Arrhenius model ($MTTF = A.e^{\frac{E_A}{KT}}$) revealed two values of negative activation energy:
  - Between -55 °C and 25 °C: Ea = -0.1 eV
  - Between 25 °C and 80 °C: Ea = -0.9 eV (N.B: Just two data points were used)



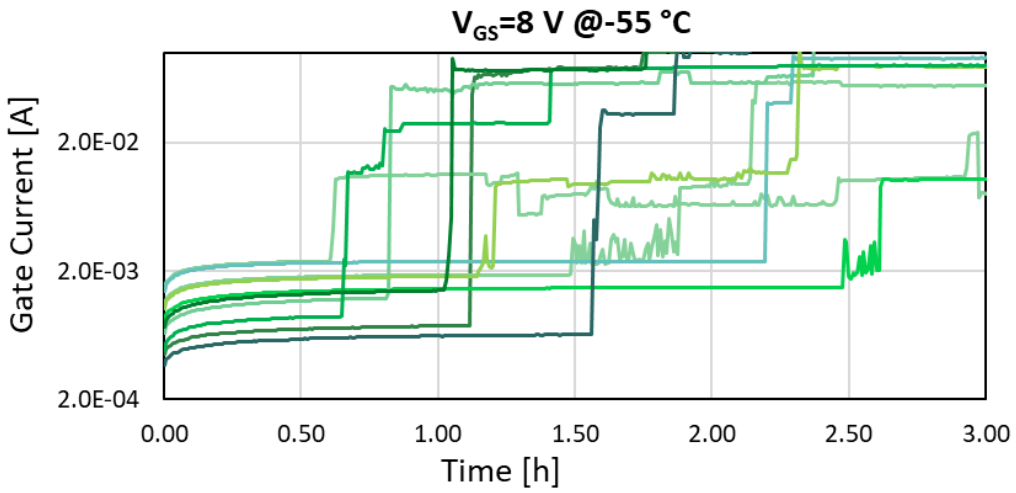


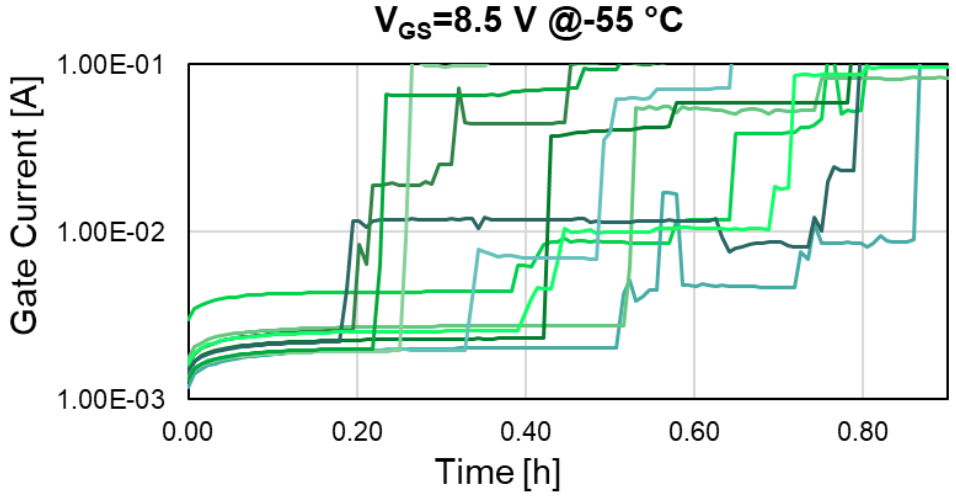
Worst case for p-GaN devices is at low temperature

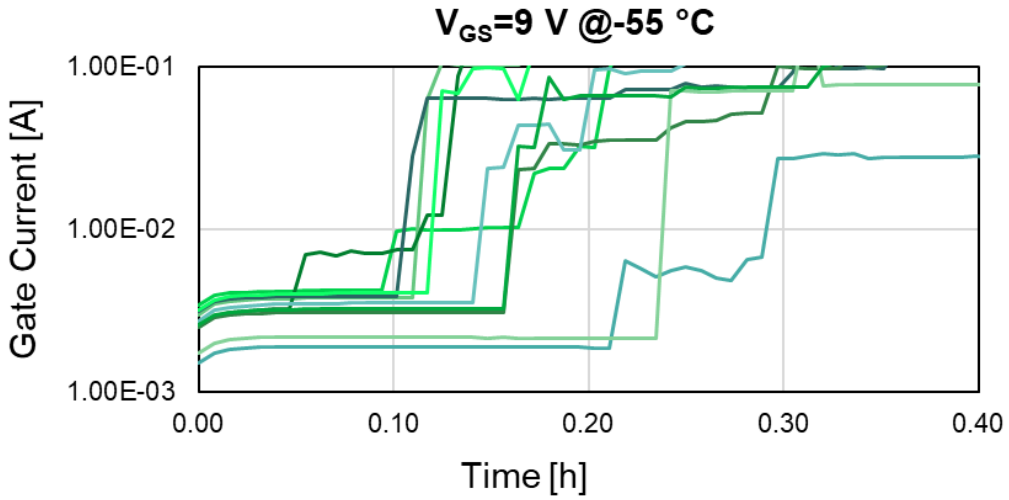
Detail results @-55°C

Influence of Vgs voltage

Results at -55 °C: Data

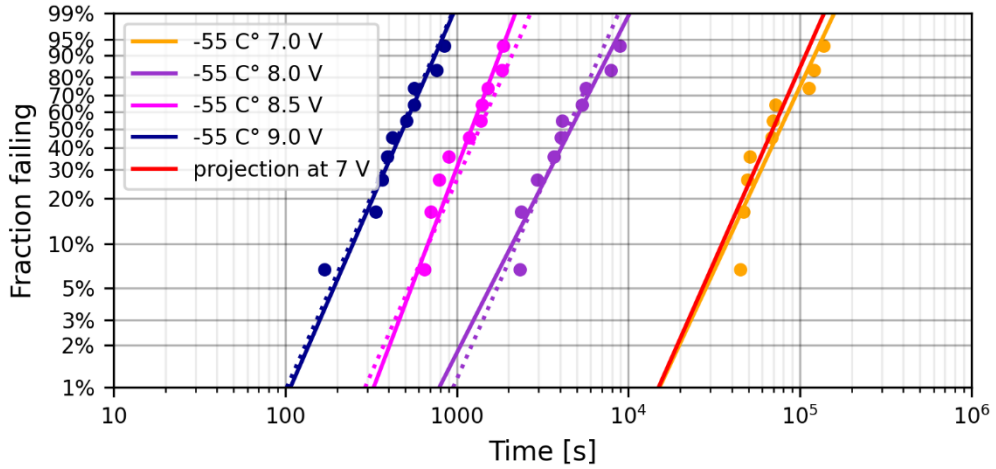


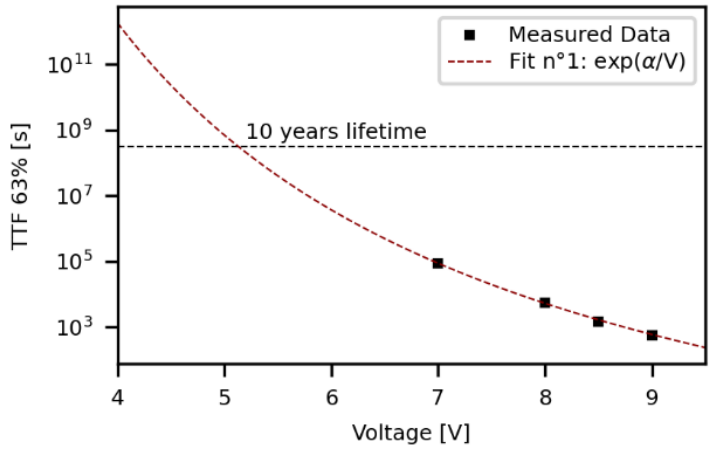




Results at –55 °C: Data

- Measurements at -55 °C were conducted to assess the effect of stress voltage and project results at 7 V (maximum rating).
- Weibull distribution results show very low TTFs at -55 °C, with an exponential model projection at 7 V estimating a TTF of ~20 hours.
- Additional measurements at 7 V confirmed the same failure mechanism between 9 V and 7 V.
- The experimental results (orange line) closely match the projected curve (red line) based on the exponential model (TTF ~ exp[α/V]).

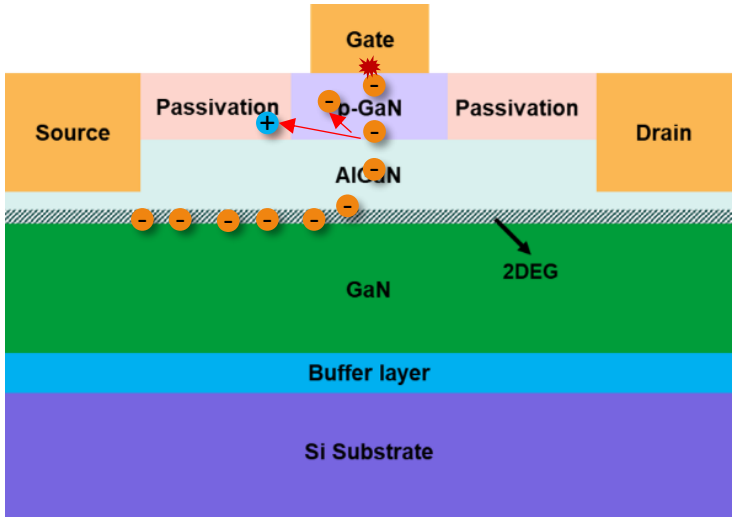


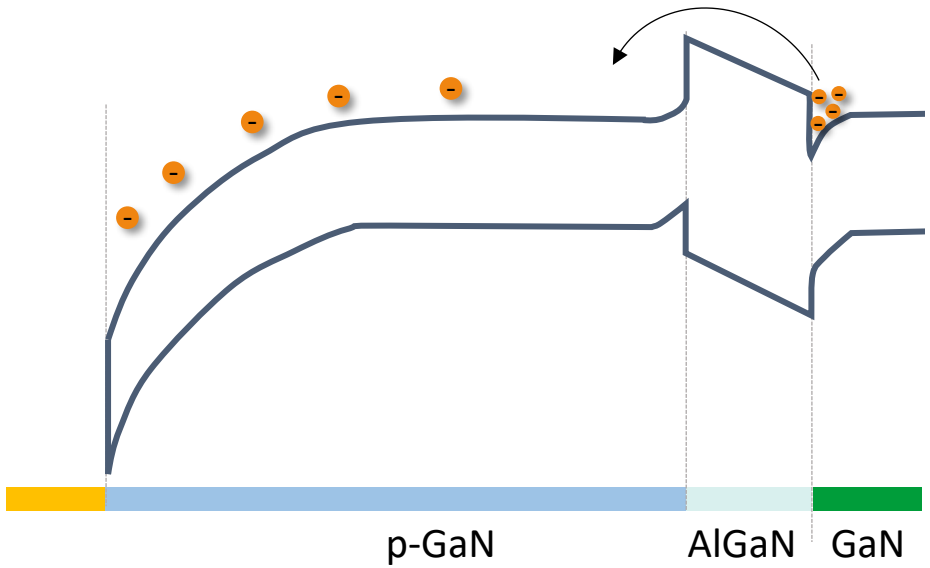


At -55 °C and 7 V, the gate lifetime is very low → To ensure a lifetime exceeding 10 years, the maximum applied voltage should be around 5V

Physical explanation

Gate Lifetime in GaN Devices, Gate Breakdown





Electrons in the 2DEG starts to spill into the p-GaN layer

Some e^- will be accelerated in the p-GaN layer

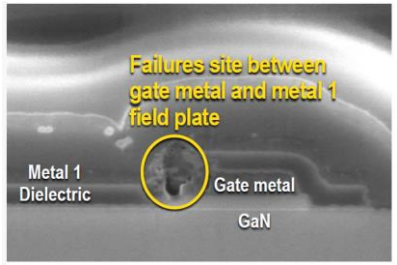
Impact Ionization

h^+ injection in the passivation dielectric

Dielectric breakdown

Damage at the metal/p-GaN layer

Schottky Contact become Ohmic



[1] J. He, G. Tang and K. J. Chen, "VTH Instability of p-GaN Gate HEMTs under Static and Dynamic Gate Stress," IEEE Electron Device Lett., vol. 39, no. 10, pp. 1576–1579, 2018,

[2] CONVERSION, EFFICIENT POWER. "GaN Reliability and Lifetime Projections: Phase 14."

Conclusion

- Accelerated lifetime tests on a commercial PGaN HEMT revealed that lower temperatures (-55 °C to 80 °C) result in shorter gate lifetimes, with measurements showing this effect above 7 V **in static bias conditions**.
- The study showed negative activation energy between -55 °C and 80 °C.
- Given that cold temperatures are the worst-case scenario, the focus was placed on -55 °C to assess the impact of applied stress voltage.
- At 7 V / -55 °C, the MTTF was approximately 20 hours, indicating that to achieve a TTF of 10 years, the applied voltage should not exceed 5 V.
- These results suggest that qualification protocols for GaN-based transistors need revision, supplementing the traditional JEDEC JESD92 tests with room temperature or below tests to ensure reliability under the most severe conditions.
- This study has been performed on one P-GaN manufacturer. A complementary study on another P-GaN manufacturer will be the subject of a new publication on Q2-2025.

Acknoledgements

GaNRET Project Industrial Secondments – Industrial & Institutional Experts –Academic Advisors - IRT personnel

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Thank you for your attention! Have you questions?

Centre Français Fiabilité

NRTW 2025

National Reliability Technology Workshop

Mercredi 19 et Jeudi 20 mars 2025 | GANIL – Bd Henri Becquerel, 14000 Caen

merci pour votre écoute !

Organisé par :